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**CDC® I/O-TTY CONTROLLER**  
**CW212-A**

GENERAL DESCRIPTION  
OPERATION  
THEORY OF OPERATION  
DIAGRAMS  
MAINTENANCE

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**HARDWARE MAINTENANCE MANUAL**





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# MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

**EXPLANATION:** Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
CW212-A	03		



# LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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# PREFACE

This manual contains the theory of operation and maintenance information for the CDC® CW212-A I/O-TTY Controller. The information presented in this manual is intended for use by maintenance personnel in training and in the field with a minimum of six months field-related experience.

Logic diagrams are not provided in this manual. The interconnecting, block, and timing diagrams presented here are intended to supplement the logic diagrams contained in the master field print package. Additional information on the I/O-TTY controller may be found in the following publications.

The Operation and Theory of Operation sections contain references to logic diagram sheet numbers and logic element location designations. Logic diagram sheet number references appear in the small boxes, located in the upper and lower right-hand corners of the boxes in the block diagram. The upper box numbers apply to the logic diagram applicable to I/O-TTY controller printed wiring board (part number 96744218). The lower box numbers apply to the logic diagram applicable to printed wiring board number 96744240. The logic element location designations are alphanumeric references that appear in the text. Designations within parentheses ( ) apply to printed wiring board number 96744218, and designations within brackets [ ] apply to printed wiring board number 96744240.

<u>Title</u>	<u>Publication Number</u>
CW212-A Field Print Package	96751200
CYBER 18 Processor with Core Memory (Macro Level) Reference Manual	88973500
CYBER 18 Computer Systems with Core Memory Installation Manual	39451500
CYBER 18 Computer Systems with MOS Memory Installation Manual	96768360



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The input/output-teletypewriter (I/O-TTY) controller performs three major functions for the CPU: it contains the teletypewriter/console display (TTY/CD) controller and the real-time clock and it contains the peripheral I/O controller data and control lines. The TTY/CD controller provides for accessing of the computer from a teletypewriter, a console display, and other RS232-C or TTL-compatible serialized input/output devices. This controller provides the basic man/machine communication interface and time lapse reference. The I/O-TTY controller and the peripheral I/O controllers provide an I/O system that is fully compatible with the CDC 1700 A/Q scheme and the National Cash Register Corp. M05 scheme of computer I/O operational systems. The CDC 1700 A/Q scheme is a read/write system that utilizes the CPU A register to transfer data and status and the Q register to transfer addresses. The NCR M05 scheme is a set/sample system that provides eight-port addressing and an eight-way priority scheme.†

## PHYSICAL DESCRIPTION

- The I/O-TTY controller is a multi-layer printed circuit board that measures 11 by 14 inches. The board contains capacitors, resistors, transistors, integrated circuits, a universal asynchronous receiver/transmitter (UART), and associated wires to produce logic, analog, and communication circuits required to provide TTY/CD, real-time clock, and peripheral I/O controller functions.

## FUNCTIONAL DESCRIPTION

- Figure 1-1 is a functional block diagram of the I/O-TTY controller. Inputs to the I/O-TTY controller consist of address and data words, micro and macro code interrupts from the CPU, keyboard codes from the TTY/CD, and data/status from the peripheral I/O controllers. The controller either outputs a data/function word to the appropriate peripheral I/O controller or processes the inputs and sends data, status, and real-time clock interrupts, or the peripheral I/O controller data/status to the CPU via the three-state bus. Display data is also sent to the TTY/CD via the associated transmission line.

Address and data words are received by the input registers from the CPU arithmetic/logical unit (ALU) (selector S3) under control of the control gate signal. All words from the CPU A and Q registers are gated into the D register of the I/O-TTY controller by the gate I/O data signal. If a word contains address information, it is gated from the D register into the Y register under control of the gate I/O address signal. The data and status (A register) words carry data and director function information to the I/O controllers and data and director status from the I/O controllers. The address (Q register) words utilize the WES/D convention (see figure 4-6) for addressing input/output data between the CPU and the peripheral I/O controllers.

† Write = set = output from CPU to I/O controller  
Read = sample = input to CPU from I/O controller

The NCR M05 set/sample scheme provides eight-port addressing and eight-level priority assignment. Each port, designated 1 through 8, can communicate with an associated peripheral device. It may also be multiplexed to communicate with up to eight peripheral devices, so that up to 64 peripheral devices can be controlled. Control of NCR equipment is implemented with the M05 set/sample I/O instructions that are included in the enhanced instruction set of the micro processor.

The contents of the address word are deciphered by the internal I/O-TTY controller logic or are applied directly to the peripheral I/O controllers. If the address selects an internal function, the I/O-TTY controller processes the data present in the D register. If the address selects a peripheral I/O controller, the data present in the D register is processed by the addressed controller. If the address selects an NCR M05 controller, the address word is processed to determine the selected port, line, mode, and device. Depending upon the mode selected, either the data present in the D register is transferred to the appropriate M05 I/O device or the data/status word is coupled through the read selection logic to the three-state bus to the CPU.

Internal I/O-TTY controller functions include a real-time clock (RTC) and a communication interface. When the real-time clock function is initiated, a macro interrupt advises the CPU that RTC has been selected and an auto-data transfer (ADT) routine is established. The CPU macro code is not to be involved in the real-time clock sequence until the selected elapsed time limit has been reached or the real-time clock has malfunctioned (lost count). The ADT routine receives the real-time clock pulse train (0.03 MHz) and processes the pulses to determine when the elapsed time limit has been reached. This real-time clock sequence is carried out independently of the CPU except for the macro interrupts.

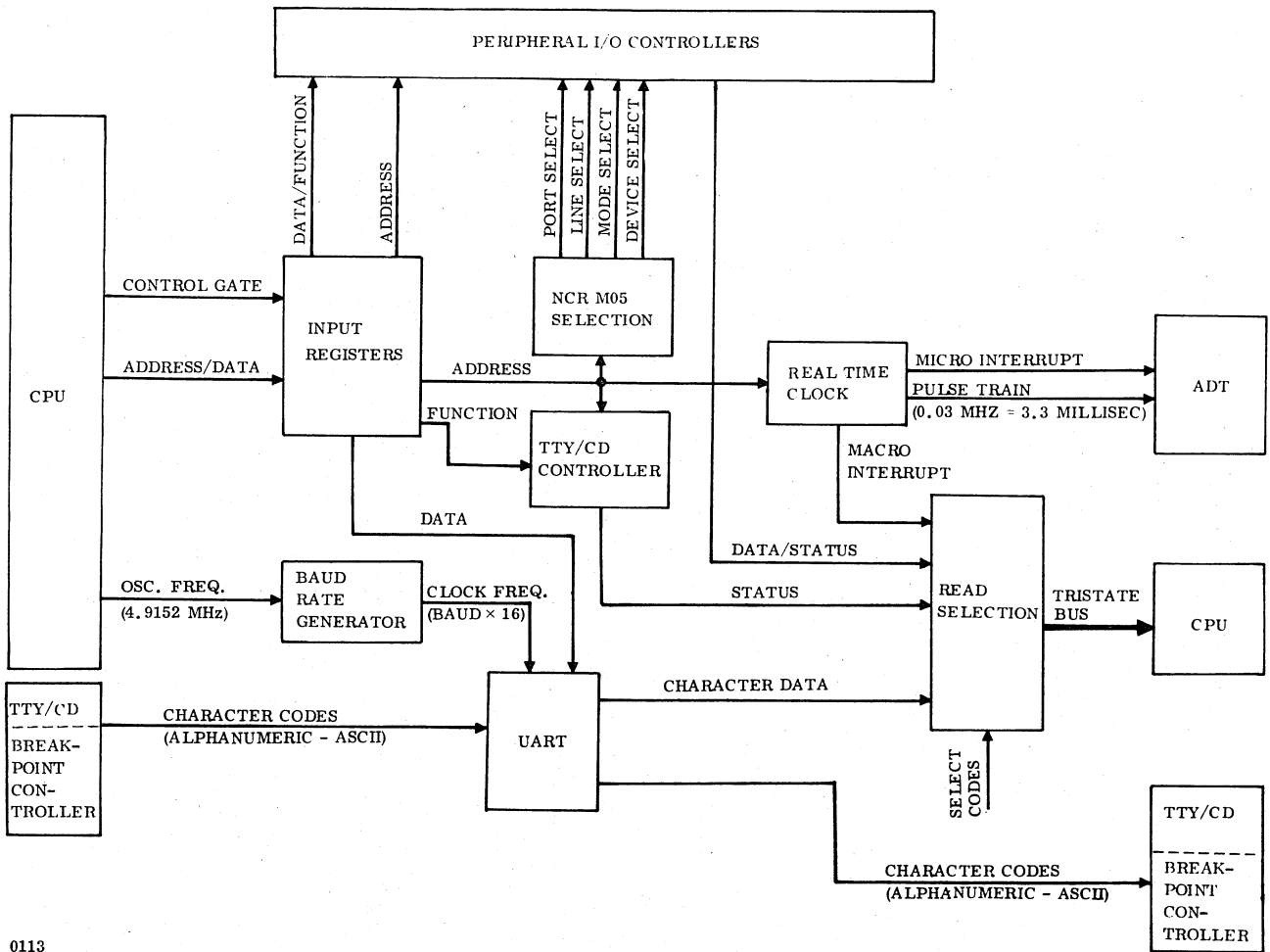
When the communication interface is selected, the character codes to and from the UART enable the conversion of keyboard characters to machine language and of machine language to character display. All CPU character data to and from the UART is transferred in parallel format, and all character codes (ASCII) are transferred between the TTY/CD and/or the breakpoint controller in serial format. Data is clocked in and out of the UART under control of the baud rate generator; the serial data is clocked at the rate of one bit every 16 baud rate clock cycles.

## REFERENCE DATA

### ELECTRICAL CHARACTERISTICS

#### Logic levels

- TTL - Low = 0 volts, high = +5 volts
- RS232-C - Excursion between  $\pm 3$  to  $\pm 12$  volts



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Figure 1-1. I/O-TTY Controller Functional Block Diagram

Transmission characteristics

- Teletypewriter - 20 mA current loop
- Console display - RS232-C
- Panel interface - TTL
- CPU to I/O - 90 kHz maximum
- Baud rates - 110, 300, 1200, 9600

PHYSICAL CHARACTERISTICS

Logic package - Dual in-line package (DIP)

Transistor package - T05 can

Modularity - Printed circuit card, four-layer

Printed circuit board size - 11 by 14 inches (279 by 356 millimeters)

ENVIRONMENTAL CONDITIONS

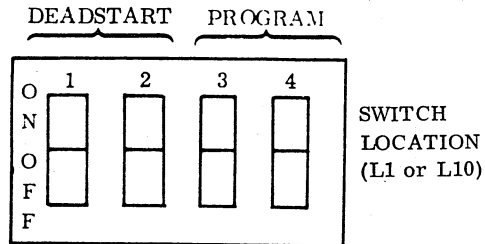
Operational:

Temperature - 40° to 120° F (4.4° to 48.4° C)  
(Maximum thermal shock 0.2° F/min.)

Relative humidity - 10 to 90 percent

The I/O-TTY controller provides a communication interface between a teletypewriter or a console display and the CPU. Communication rates vary with the device and the application, so the rate select switch at location (L10) [L1]

(figure 2-1) must be set to the correct rate for the device attached. The basic rate is 9600 baud, but a rate of 110, 300, or 1200 baud may be selected.



### BAUD RATE SELECTION

Rate	Deadstart		Program	
	Switch Position 1	Switch Position 2	Switch Position 3	Switch Position 4
110	ON	ON	ON	ON
300	ON	OFF	ON	OFF
1200	OFF	ON	OFF	ON
9600 †	OFF	OFF	OFF	OFF

† Normal Operating Position

Figure 2-1. I/O-TTY Controller Switch



# INSTALLATION AND CHECKOUT

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Information for this section is contained in the CYBER 18  
Computer Systems Installation Manual.



This section contains the external and internal signal interface diagrams and tables. The diagrams depict the source and termination, and the tables define all the write and read data and control signals that enter and leave the I/O-TTY controller. Detailed descriptions of the internal I/O-TTY controller functions are illustrated by block diagrams. These diagrams contain blocks that represent groups of logic that perform functions: numbers in the upper right corner of these blocks indicate the field print package logic diagram sheet that contains the functional logic group. Also provided is a detailed chip-by-chip description of the logic conditions that produce the required effects to provide the I/O-TTY controller operations.

## EXTERNAL INTERFACE

Figures 5-1 and 5-2 indicate the source and termination points of data and control signals applicable to the I/O-TTY controller. Tables 4-1 and 4-2 tabulate these signal names in alphabetical sequence and provide a source, description, and application description of each.

The field print package logic diagrams contain diagonal (/) and bar (̄) symbols to indicate an active low (not) condition of the signal. The diagonal is used to designate the low condition of external read and write signals and the bar is used to designate the low condition of internal signals (for example, SD01/ through SD16/, ADR01/ through ADR16/; D01 through D16, Y01 through Y16).

## OVERALL FUNCTIONAL DESCRIPTIONS

The I/O-TTY controller contains all the logic for the program control of data to and from the computer peripheral I/O controllers (A/Q and M05); of the internal TTY/CD control, data, and status, and generation of the real-time clock elapse time base and interrupts. This controller, in conjunction with the basic micro processor, 1700 emulator, and peripheral I/O controllers, provides an I/O technique that is fully compatible with the 1700 A/Q and M05 I/O schemes.

The A/Q scheme utilizes standard Control Data data/address word and reply/reject conventions to process and address I/O data within the processor (figure 4-1). Figure 4-2 illustrates the overall TTY controller timing.

The M05 scheme employs a set/sample (write/read) technique whereby the data is placed on the input/output line and remains until a strobe pulse occurs within the I/O timeframe (figure 4-3).

## PERIPHERAL I/O CONTROLLERS

The data signal flow block diagram for the I/O-TTY controller is presented in figure 4-4. Figure 4-5 is the control line signal flow block diagram.

## 1700 COMPUTER A/Q SCHEME

All write data and address words transferred from the CPU to the peripheral I/O controllers are coupled through the I/O-TTY controller D and Y input registers. The D register holds false (complement) data; it couples the data words from the CPU A register to the peripheral I/O controller via the send lines (SD01 through SD16). The Y register holds true data; it couples address words from the CPU Q register to the peripheral I/O controllers via the address lines (ADR01 through ADR16). (Y register bits ADR12 through ADR16 are low only when the transfer (ADT) mode of operation has been selected.)

The data and address words are gated into the respective registers under control of the D' micro instruction (000 = gate I/O data, 001 = gate I/O address). The D' micro instruction is a 56-nanosecond negative-going pulse that strobes data from the CPU arithmetic/logical unit (ALU) into the D register when the leading edge swings negative. If D' is equal to 001, the data is strobed from the D register to the Y register when the trailing edge of the gate poke swings positive. All read data is transferred via the open collector lines (RD01 through RD16) to the data read multiplexers. The read data is then transferred to the CPU three-state bus via bus lines BUS00 through BUS15 under control of the program-controlled data read multiplexers.

## M05 Set/Sample Scheme

The M05 set/sample scheme provides program-controlled selection of the active I/O port, line, device, and mode. The selection is deciphered from the contents of the port select (SPT00 through SPT07), line select (SSEL00 through SSEL07), position select (SPOS01 through SPOS03), and mode select (SMB07 through SMB09) lines.

The address word in the Y register is decoded in accordance with the CDC 1700 Series WES/D convention (figure 4-6).

The contents of the Y register indicate the selections as shown in figure 4-7.

The send port selection is designated by the octal value of Y-register bits 8 through 10 when Y11 is low. The line selection is designated by the octal code value of bits Y08 through Y10 when Y11 is high. The position (device) selection is designated by the octal code value of bits Y05 through Y07. The mode selection is determined by the state of bit Y04 (SMB09). When Y04 is high, the set mode is selected, placing the data word (16 bits) in the D register on the send lines (SD01 through SD16). When Y04 is low, the sample mode is selected; the data word on read data lines RD01 through RD16 is transferred via the open collector bus to the program-controlled data read multiplexers. The data is placed on the CPU three-state bus via bus lines BUS00 through BUS15 under control of the data read multiplexers.

Y register bits 5 through 16 determine whether the M05 set/sample scheme has been selected. This is indicated when the address word W-field bits (Y12 through Y16) are all low (W = 0), the E field (Y08 through Y11) hexadecimal value is greater than 8, and the S field (Y05 through Y07) is selecting a device.

TABLE 4-1. EXTERNAL DATA SIGNALS

Signal	Source	Application
ADR01/ through ADR16/ (ARD01 = LSB)	Y register (extension of Q register data)	Transfer of address data to peripheral I/O controller; the nine highest order bits specify the device, and the seven lowest order bits specify the function
BUS00/ through BUS15/ (BUS00 = MSB)	Read register	Transfer of real-time clock status, TTY controller status, character data, or peripheral I/O controller data to CPU via three-state bus
RD01/ through RD16/ (RD01 = LSB)	Peripheral I/O controllers	Transfer of peripheral I/O controller data and status to CPU three-state bus
RS232IN-1	Console display (CD)	Transmission of CD or breakpoint controller character codes (ASCII) to CPU via I/O-TTY controller; signals must conform with EIA standard RS232-C and CCITT recommendation V24
RS232IN-2	Not used	
RS232OUT-1	I/O-TTY controller	Transmission of character codes from CPU to CD or breakpoint controller; signals must con- form to EIA standard RS232-C and CCITT recommendation V24
RS232OUT-1	Not used	
S300/ through S315/ (S300 = MSB)	Selector S3 of ALU	Transfer of address, director functions, or data to the I/O controllers
SD01/ through SD16/ (SD01/ = LSB)	D register (extension of A register data)	Transfer of director functions or data to peripheral I/O controllers
SMB07/ through SMB09†	Y-register bits 2 through 4 (ADR02 through ADR04)	Transfer of mode bits to M05 device
SPOS01/ through SPOS03/†	Y-register bits 5 through 7 (ADR05 through ADR07)	Bits that specify the position of the M05 device on the port; up to eight multiple devices may be on the same port
SPT00/ through SPT07/†	I/O-TTY controller	M05 port selection signals (hexadecimal code selection of port address lines); the active line is determined by the E bits of the Y-register address word. These lines are custom-wired to the associated M05 controller port at time of installation.
SSEL00/ through SSEL07/†	I/O-TTY controller	M05 peripheral device selection in accordance with ADT operations
TTL-SRL-1	M05 (set/sample) I/O devices, TTY, or panel interface	Transmission of M05 I/O device data to the I/O-TTY controller from the CPU
TTL-SRL-2	I/O-TTY controller	Transmission of M05 data from I/O-TTY con- troller to the CPU
I/OTTYIN	Teletypewriter	Transmission of teletypewriter character codes (ASCII) over a 10 mA current loop from CPU to I/O-TTY controller
TTYUARTOUT	I/O-TTY controller UART	Transmission of teletypewriter character codes (ASCII) over a 20 mA current loop from I/O-TTY controller to teletypewriter

† Applicable to M05 set/sample peripheral controllers only.

TABLE 4-2. EXTERNAL CONTROL SIGNALS

Signal	Source	Application
AUTO-DATA	Status/mode interrupt (SMI) module in CPU	Micro level memory transfer of data blocks to or from any device that can accommodate the ADT mode of operation; the 1700 emulator processes each data interrupt and inputs or outputs the next word of data
CHAR INPUT	I/O-TTY or other I/O controller	Sent by the I/O controller(s) to the CPU during read operations; when the line is active, an 8-bit character code is loaded into the lower eight bits of the A register without disturbing the upper eight bits of the A register.
CPUEDS	Memory	Indication from memory that data has been received
CPUPROT/	Transform	A discrete signal that indicates the CPU is in a protected status and only those instructions containing a 0 in the protected bit position will be accepted. All other are rejected.
DS-SW-NC DS-SW-NO	External deadstart switch (customer-supplied)	When connected, provides for external loading of data into the CPU. (NC = normal closed; NO = normal open; requires momentary double-pole single-throw contact arrangement)
DSUARTCLK/	I/O-TTY controller	153.6 kHz clock signal which is 16 times the maximum baud rate of 9600; sent to the card reader/line printer controller
ENABLEIO/	Control 1 module in the CPU	Enables transfer of I/O-TTY controller and peripheral I/O controller data to the three-state bus
ENMMWRITEPNL/	Breakpoint controller	Breakpoint controller switch condition that provides for input of data to micro memory
ENMMWRITE	I/O-TTY controller	Provides for input of data to micro memory via control 1.
EXSTOP/	I/O-TTY controller	An interrupt signal that initiates a processor macro stop (clear SM204), which causes emulation to stop
GATEIOADR/	Control 1	A 56-nanosecond negative-going pulse that strobes D-register data to the Y register (executed by micro instruction D'=001, establishing that this is I/O address data) coincident with trailing edge transition
GATEIODAT/	Control 1	A 56-nanosecond negative-going pulse that strobes ALU data to the D register (executed by micro instruction D=000, establishing that this is I/O data) coincident with leading edge transition
MC/	Control 1	A discrete signal developed by the CPU whenever a processor master clear occurs; it is used to clear the I/O channels and external equipment
MCDELAYED/	Control 1	A delay of master clear until the protected areas have been inhibited from clearing operation.
MC-S/	I/O-TTY controller	Master clear request condition sent to control 1 to initiate a master clear.

TABLE 4-2. EXTERNAL CONTROL SIGNALS (Contd)

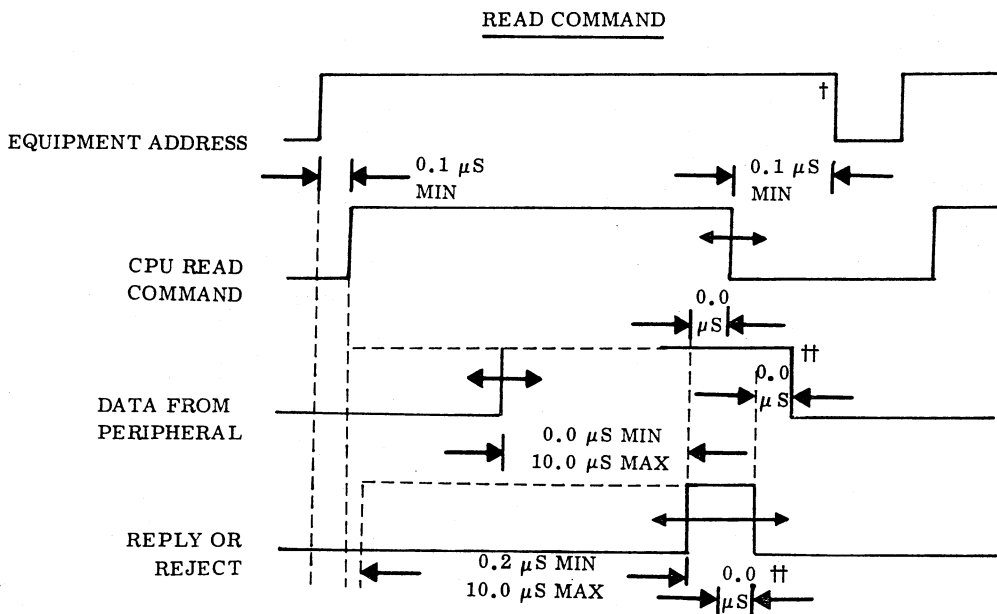
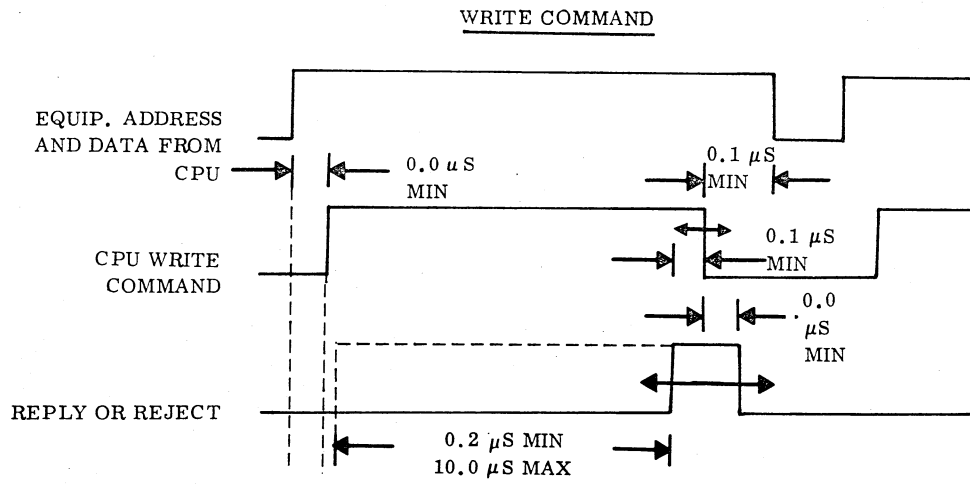
Signal	Source	Application
MC-SW-NC MC-SW-NO	External master clear switch (customer-supplied)	When connected, provides for initiating the master clear condition that returns CPU to the initialization routine (NC = normal closed; NO = normal open; requires momentary double-pole single-throw contact arrangement)
MICROSTRT/	I/O-TTY controller	I/O-TTY controller logic that enables micro-start when panel interface is not supplied
MIR12	Control 1	Micro instruction register bit 12 provides selection response control (character input, reply, reject, RTERM) responses to the CPU via the three-state bus
MI-SW-NC MI-SW-NO	External manual interrupt switch (customer-provided)	When connected, provides application of CPU manual interrupt (NC = normal closed; NO = normal open; requires momentary double-pole single-throw contact arrangement)
MR/	CPU	Originates in the CPU as a master clear and clears I/O controllers and external equipment
MULTIND/	I/O-TTY controller	Panel simulation selection of indirect addressing capabilities
MULTINDPNL/	Breakpoint controller	Breakpoint controller switch that provides for jump from the present address to auxiliary addresses
OSC. 4.9152 MHz	Control 2	Fundamental oscillator frequency source from which the baud rate generator, timing generator, and real-time clock rates are derived
PNBAUD00/ PNBAUD1/	I/O-TTY controller	Baud rate clock frequency selection for the panel interface
PNLPRES/	Breakpoint controller	A discrete low (ground) signal produced when the breakpoint controller is inserted
PNLMODENA	External	Allows entering into the reserve (panel) mode (by pressing the escape button on the TTY/CD) when high, and prevents entering into the reserve (panel) mode when low. When no connection is made to this signal, entering into the reserve mode is allowed.
PN-TTL-OUT	Transmission line for transfer of TTL level data to the breakpoint controller	Provide for transmission of keyboard character code via TTL levels to the breakpoint controller
PROG-PROT/	I/O-TTY controller	Indicates to I/O controllers that I/O instruction is protected
PROTECT/	I/O-TTY controller	Protect switch to the transform
PROTECTPNL/	Panel interface function control register	Enables CPU protect system when panel interface is present
RDINT01/	I/O-TTY controller	Interrupts CPU whenever TTY is ready to transfer a byte of data during auto-data transfer
RDINT08/	Real-time clock	Micro level interrupt that occurs every 3.33 milliseconds when real-time clock is enabled
RDINT12/	I/O-TTY controller	Micro level interrupt that occurs whenever a panel key is pressed during panel simulation operation
RDINT13/	I/O-TTY controller	Interrupt to the SMI to indicate the TTY/CD controller UART transmit buffer register is empty during panel simulation

TABLE 4-2. EXTERNAL CONTROL SIGNALS (Contd)

Signal	Source	Application
READ-SSTB/	SMI	A strobe signal for the M05 peripheral controller; occurs twice with each execution of set/sample input/output (SIO) command; occurs once near the beginning and once near the end of an output data operation
REJECT	I/O-TTY or other I/O controller	If the specified operation cannot be performed by the I/O when the read or write signal appears, a reject response is sent to the CPU within 10 microseconds. If no I/O response (reply or reject) occurs within 13 microseconds after the request, the emulator generates an internal reject.
REPLY	I/O-TTY or other I/O controller	Indicates to the CPU that the associated I/O device is available to send or receive data. Write event sequence: <ol style="list-style-type: none"> <li>1. CPU bus (internal A/Q channel) transfer data to the appropriate register of the peripheral device.</li> <li>2. The peripheral device sends a reply signal to the A/Q channel a maximum of 10 microseconds later.</li> <li>3. The A/Q channel drops the write signal when the reply is received.</li> <li>4. Absence of a write signal drops the reply</li> </ol> Read event sequence: <ol style="list-style-type: none"> <li>1. Available data is gated onto the input bus.</li> <li>2. Reply is executed a minimum of 200 nanoseconds and a maximum of 10 microseconds.</li> <li>3. Reply causes the read signal to drop.</li> <li>4. Absence of a read signal drops the reply signal.</li> <li>5. The data line signal drops when the reply signal drops.</li> </ol>
RESYNC I/O	Control 1	Strobe pulse that enables the transfer of I/O-TTY controller and peripheral I/O controller response
RPINT17/	I/O-TTY controller	Macro level signal that signals end-of-operation alarm, or manual interrupt
RPINT24/	Real-time clock within the I/O-TTY controller	Macro level signal that signals termination of the real-time clock operation
SELGETMAK/	Transform	Micro level signal used for step mode during panel simulation
SELSKIP/	I/O-TTY controller	Selects the skip condition for the selective skip instruction
SELSKIPNL/	Breakpoint controller	Skip switch condition from the panel
SELSTOP/	I/O-TTY controller	When active, causes the CPU to halt when a selective stop instruction is encountered

TABLE 4-2. EXTERNAL CONTROL SIGNALS (Contd)

Signal	Source	Application
SELSTOPNL/	Breakpoint controller	Stop switch condition from the panel
SET SM204/	I/O-TTY controller	Initiates the deadstart routine
SM204/	SMI	Micro-level signal that selects deadstart baud rate selection for the panel interface
SM210/, SM211/	SMI	Status mode register 2 outputs
SM212/	Not used	
STERM/	SMI	A signal that the emulator generates when the last transfer of a current automatic data transfer (ADT) operation is in progress
WE0/	I/O-TTY controller	W equals zero (Y-register W field hexadecimal value of an address word). This signal is present whenever bits 12 through 16 of the address in the Y register are all low.
WRITE	SMI	Initiates an output transfer of one data word from the ALU A register to the I/O-TTY controller D register

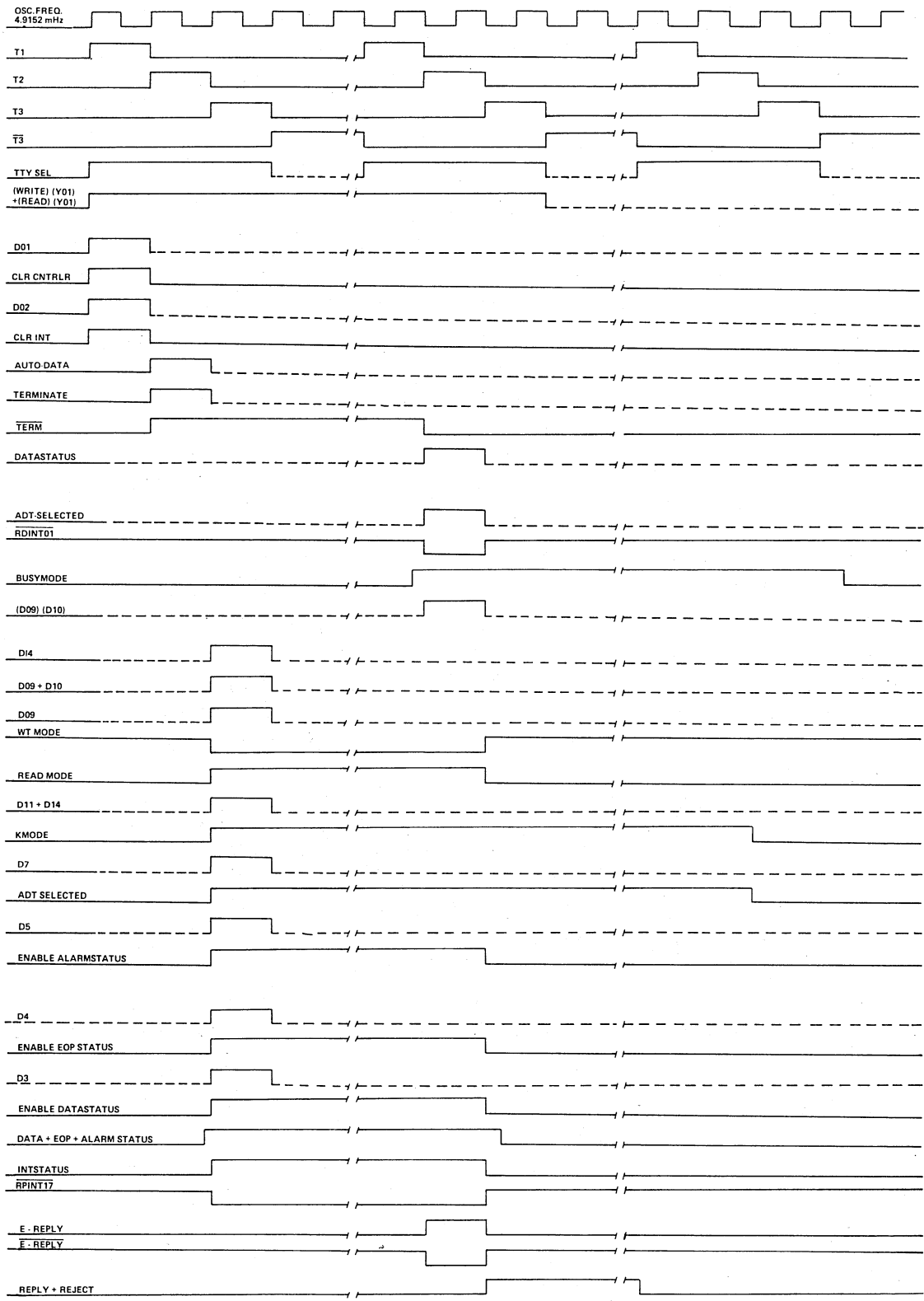


† ADDRESS AND DATA LINES NEED NOT DROP AFTER THE CPU READ COMMAND DROPS, AND IN GENERAL, THEY WILL NOT CHANGE UNTIL THE BEGINNING OF THE NEXT I/O OPERATION.

†† THERE ARE NO MAXIMUM TIMES SPECIFIED FOR THESE EVENTS BUT IT IS ESSENTIAL THAT THEY BE KEPT TO AN ABSOLUTE MINIMUM. THEREFORE, IT IS STRONGLY RECOMMENDED THAT COMBINATIONAL LOGIC BE USED TO CONTROL THESE SIGNALS.

0114

Figure 4-1. A/Q I/O Timing



0119

Figure 4-2. Overall TTY Controller Timing

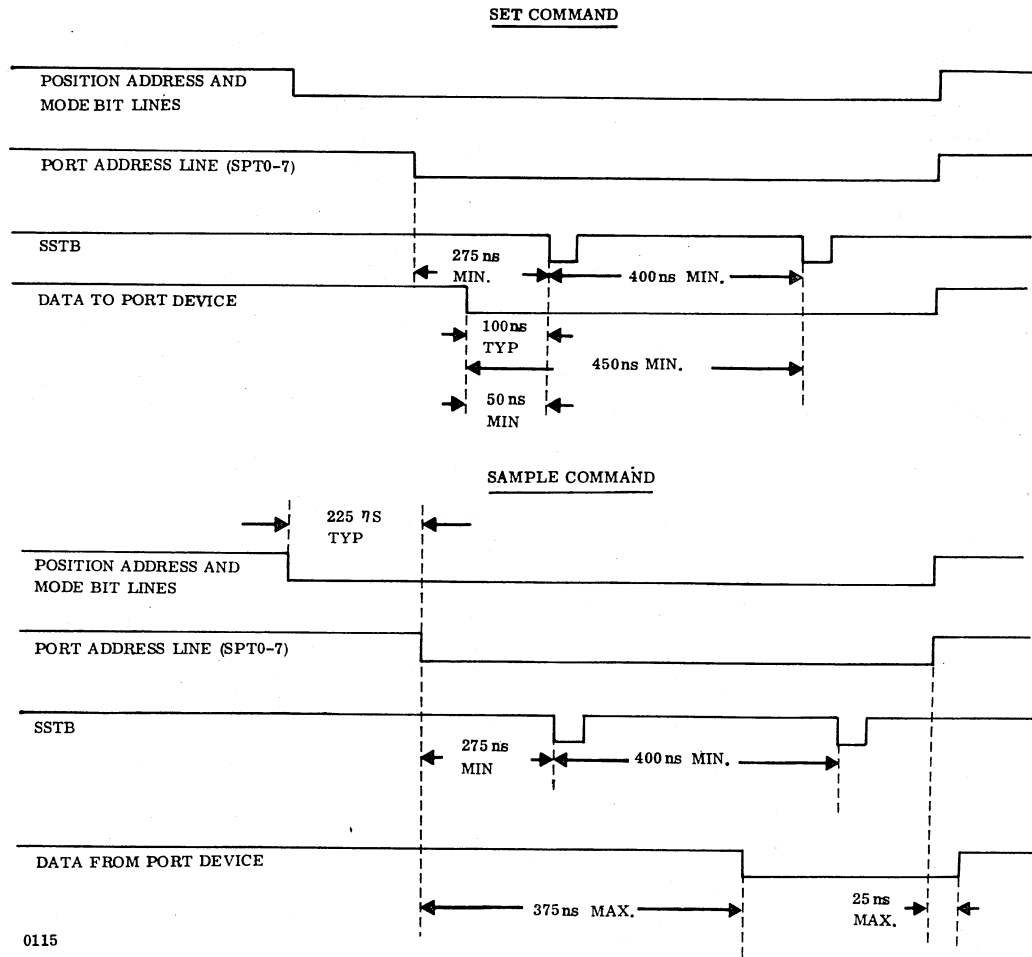
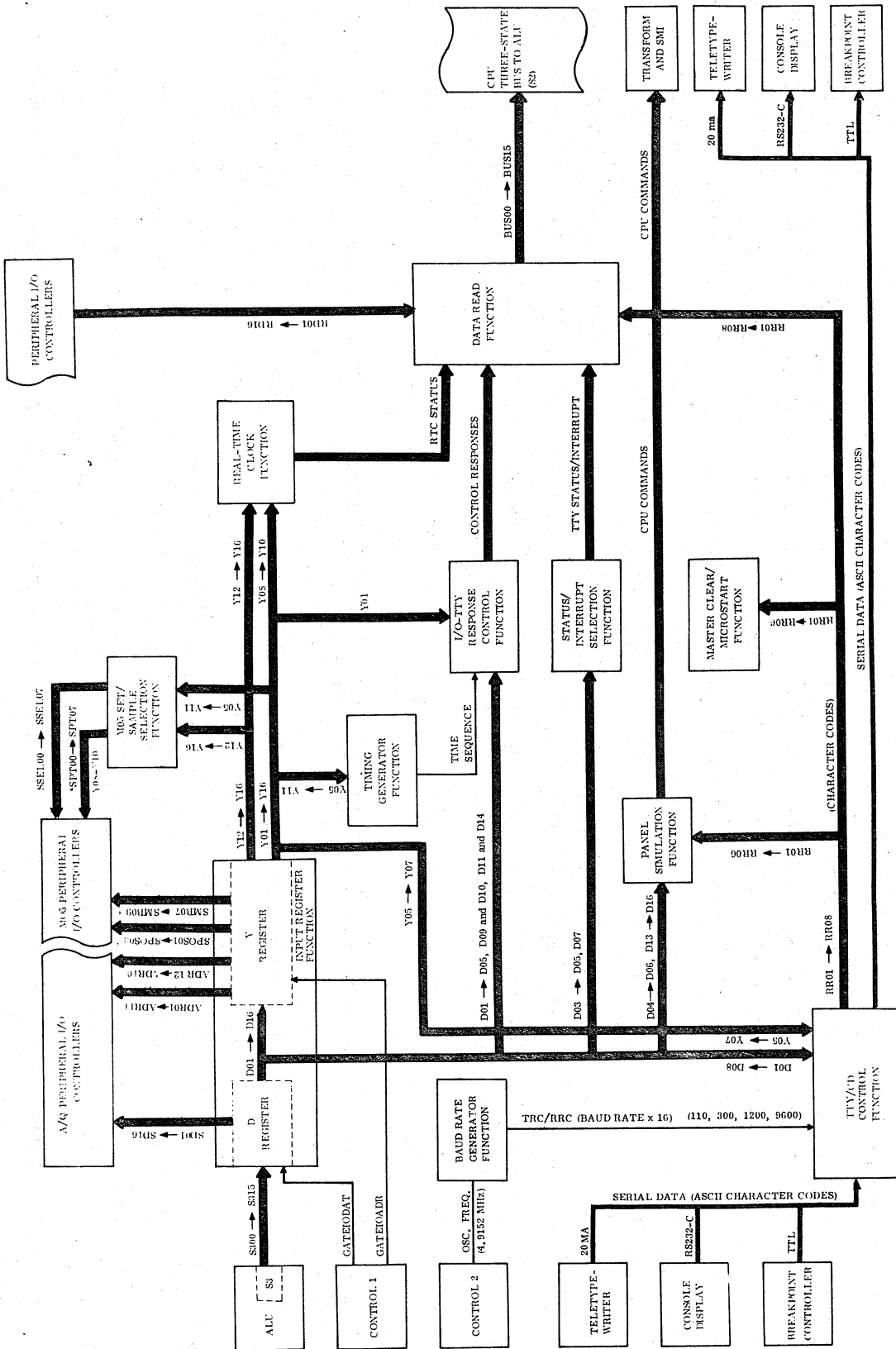


Figure 4-3. M05 I/O Scheme Timing



- NOTES:
1. DESIGNATIONS APPLICABLE TO M05 SET/SAMPLE CAPABILITY ONLY WHEN CUSTOM WIRED.
  2. PARALLEL DATA TRANSFER
  3. SERIAL DATA TRANSFER
  4. CONTROL LINE

0121

Figure 4-4. I/O-TTY Controller Data Signal Flow Block Diagram

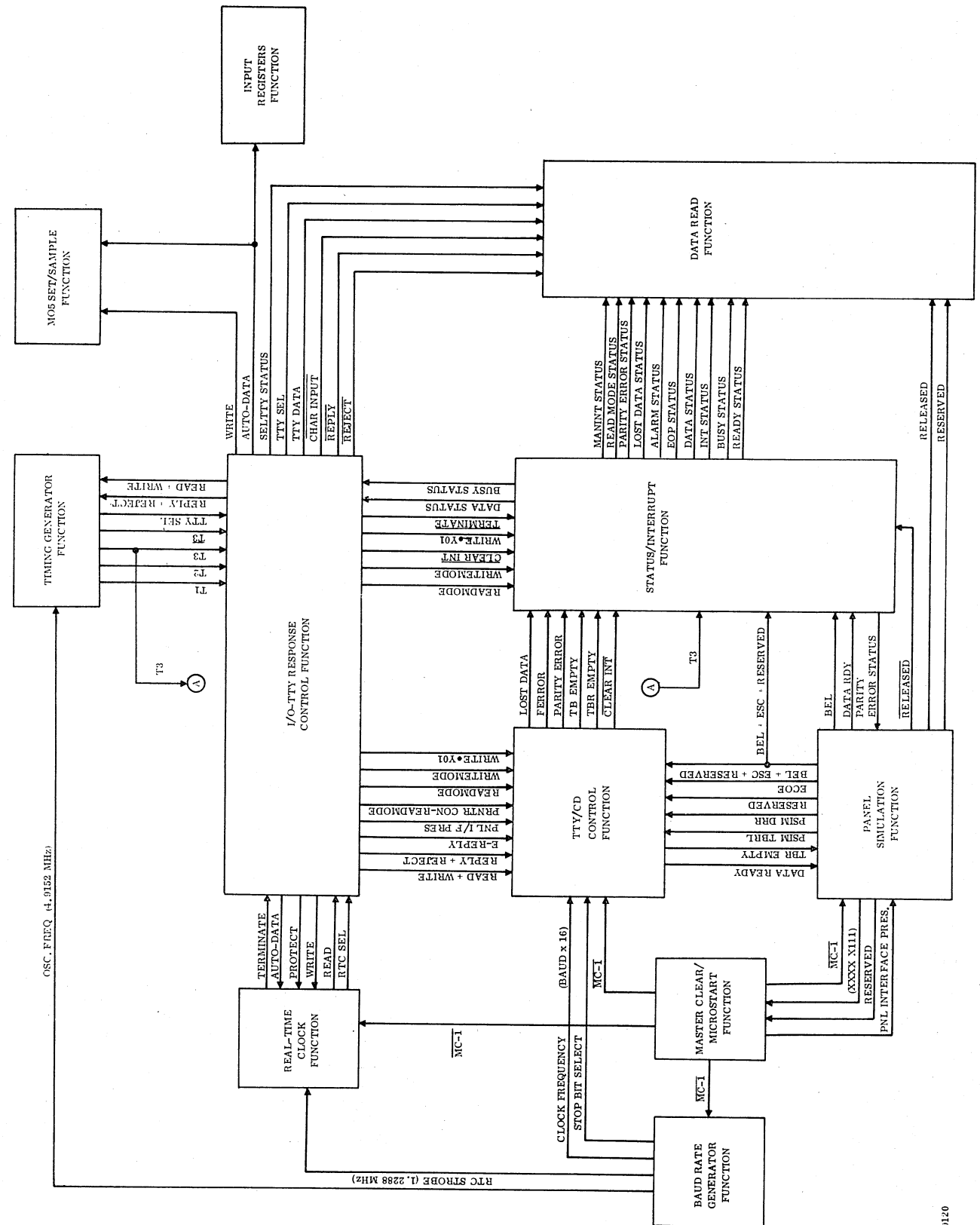


Figure 4-5. I/O-TTY Controller Control Line Flow Block Diagram

0120

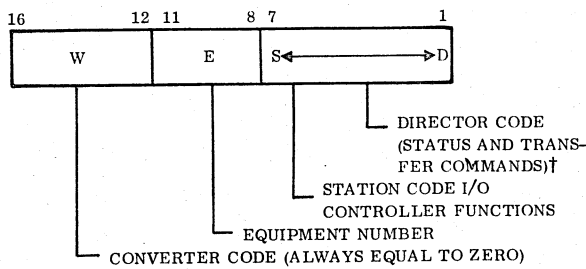


Figure 4-6. WES/D Convention

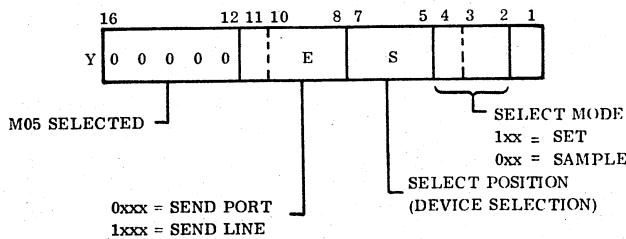


Figure 4-7. Y Register Set/Sample Selections

## INTERNAL I/O CONTROL

The internal TTY/CD control logic provides the data paths and control signals required for the man/machine communication link with the CPU. Y-register bits are applied to the timing generator and I/O-TTY response control functions to produce the time segment that ensures data transfer, reply, or reject responses are properly timed. The timing generator employs Y-register bits 5 through 7 to ensure that the TTY selected (TTYSEL) condition exists before generating time periods T1, T2, T3, and T3. The I/O-TTY response control function uses Y-register bit 1 to determine the write and read mode responses. (The real-time clock is described later in this section.)

The D register data bits are applied to the I/O-TTY response control, status/interrupt selection, panel simulation, and TTY/CD control functions to designate the director function and provide the character codes to the peripheral device. The I/O-TTY response control function deciphers the D register to determine the function designated, and the response provided agrees or disagrees to produce the proper reply or reject control response. Bits D03 through D05 and D07 indicate to the status/interrupt selection function the appropriate status and interrupt response. Bits D04 through D06 and D13 through D16 indicate to the panel simulation function the appropriate CPU command. D-register bits 1 through 8 are sent to the TTY/CD control function to provide character codes to the teletypewriter, console display, and/or breakpoint controller. The character code data bits are applied to the TTY/CD control function in parallel format and are strobed out to the teletypewriter, CD, and/or breakpoint controller in serial format, under control of the baud rate generator, at the rate of one bit per 16 Hz of clock frequency.

Character codes (ASCII codes) can be injected into the CPU from the teletypewriter, CD, or breakpoint controller. The character codes are clocked into the TTY/CD control function by the baud rate generator, where they are converted to parallel format (RR01 through RR08) and applied to the panel simulation, master clear/microstart,

and data read functions. The panel simulation and master clear/microstart functions decipher the character data (RR01 through RR06) to provide the reserve (ESC), release (@), manual interrupt (BEL), and master clear (?) commands selectable at the keyboards. The data applied to the data read function is gated onto the CPU three-state bus.

The real-time clock decodes Y register data to determine whether the real-time clock function has been selected. The actual elapsed time pulses (3.3 ms) are processed by the ADT logic and only the status signals are coupled to the CPU.

The real-time clock status, control response, TTY status/interrupt, read data (RD01 through RD16), and character data (RR01 through RR08) conditions present at the data read function are multiplexed to the CPU three-state bus. Selection conditions applied to the data read function multiplexer indicate the transfer of one of the five data conditions to the bus lines (BUS00 through BUS15). These bus lines place the selected data conditions on the CPU three-state bus.

## DETAILED FUNCTIONAL DESCRIPTIONS

### INPUT REGISTERS FUNCTION

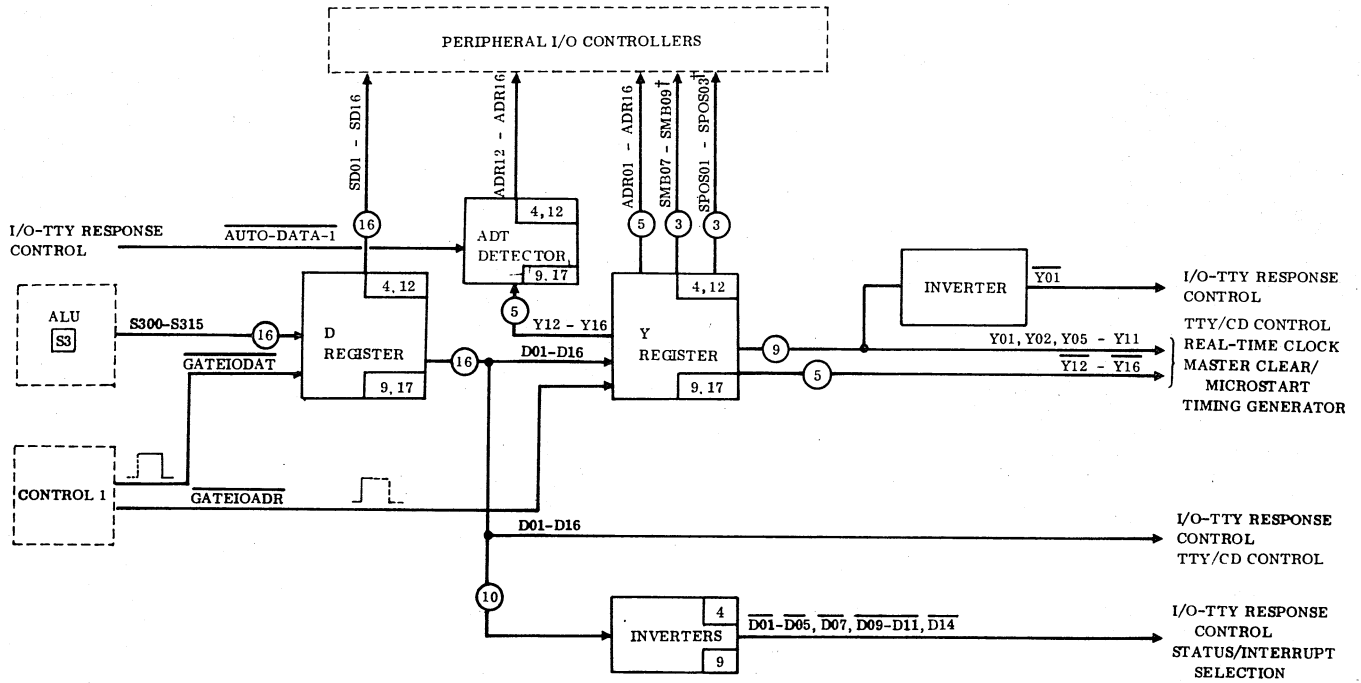
The input registers function is shown in figure 4-8.

The I/O-TTY controller input registers receive data and address words from the CPU via selector 3 of the ALU for use in the I/O-TTY and peripheral I/O controllers. The registers are designated D (data) and Y (address) and are direct extensions of the CPU A and Q registers, respectively. The D register is loaded by execution of the CPU micro instruction D', which initiates a control signal within the control 1 module that produces the gate I/O data and gate I/O address signals. These signals gate data and address words into the I/O-TTY controller.

When D' equal 000, the GATEIODAT signal goes low and the data word is transferred from the ALU, selector 3, into the D register via lines S300 through S315. If it is a data word, D01 through D16 and SD01/ through SD16/ (flip-flops A11, C11, E11, and G11) [flip-flops A10, C10, F10, and F9] are set according to the input word bit settings to apply the D-register director functions or character data to the I/O controllers. Figure 4-9 illustrates the I/O-TTY controller director functions.

When D' equals 001, the GATEIOADR signal goes high and the word residing in the D register is transferred to the Y register (flip-flops B11, D11, F11, and H11) [flip-flops A9, C9, G10, and F8]. The data bits of the address word set output lines ADR01 through ADR16 and internal lines Y01 through Y16 low and high to impose the address word contents upon the peripheral I/O controllers and I/O-TTY controller functions. Outputs Y12 through Y16 and ANDed at gates (L9 and H11) [L10 and G8] with the automatic data transfer (AUTO-DATA-1) signal to force the W field equal to zero during an ADT operation and produce the ADR12/ through ADR16/ signals.

Bits D01 through D05, D07, D09 through D11, and D14 are inverted at (A8, A4, E8, and G4) [A8, C8, M4, and D4] to provide the complement signal to the internal logic and to avoid applying the internal load to the associated output lines (SD01 through SD16). Bit Y01 is inverted to provide both the true and complement signals to the internal functions.



DESIGNATIONS APPLICABLE TO M05 SET/SAMPLE CAPABILITY ONLY.  
079

Figure 4-8. Input Registers Function

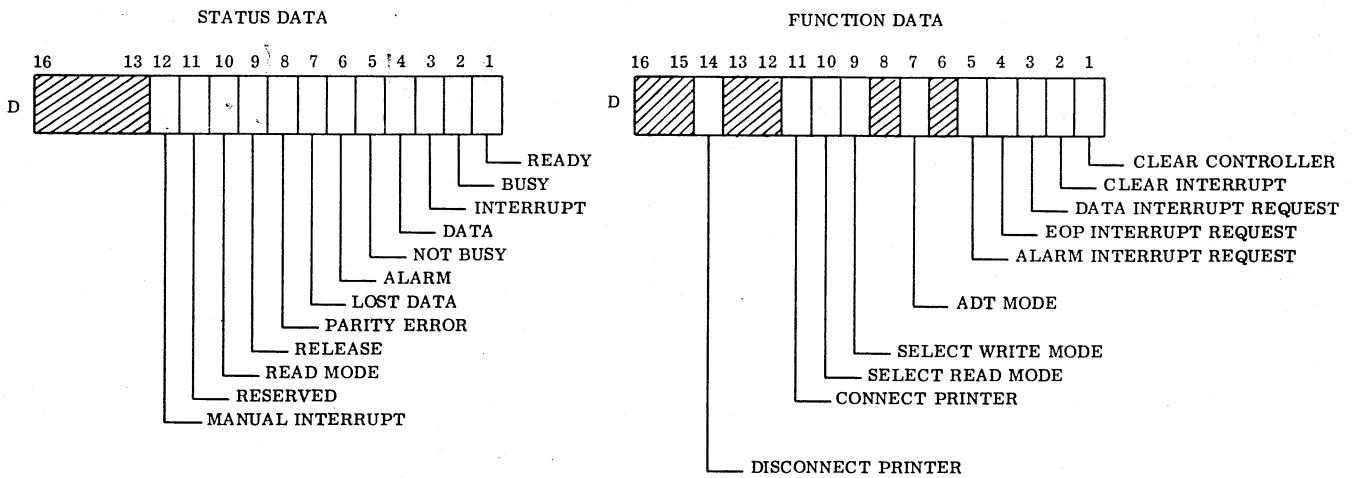


Figure 4-9. D Register Bit Definitions, Director Data

When M05 set/sample capabilities are provided, output lines ADR02 through ADR04 and ADR05 through ADR07 are designated SMB07 through SMB09 and SPOS01 through SPOS03, respectively. The SMB and SPOS lines control the M05 operating mode and the port selection of M05 peripheral devices. When SMB09 is set, the 16 bits of information contained in the data register are placed on output lines SD01 through SD16. When SMB09 is 0, the 16 bits of information on input lines RD01 through RD16 are transferred via the I/O-TTY controller to the three-state bus. Bits SMB07 and SMB08 are not defined and may be employed at the user's discretion. The octal code designation of the selected port, SPOS01 through SPOS03, is transmitted on the port line SPT.

### I/O-TTY CONTROL RESPONSE FUNCTION

The I/O-TTY control response function (figure 4-10) provides the I/O-TTY controller control responses (reply, reject, character input, and enable reply) to the CPU three-state bus via the data read function. It also provides the I/O-TTY controller auto-data transfer interrupt signals (RDINT01) to the SMI for incrementing the TTY ADT table sequences, and controller internal signals (SELTTYSTATUS, AUTO-DATA, REPLY+REJECT, and clear interrupt) for processing within the associated function logic.

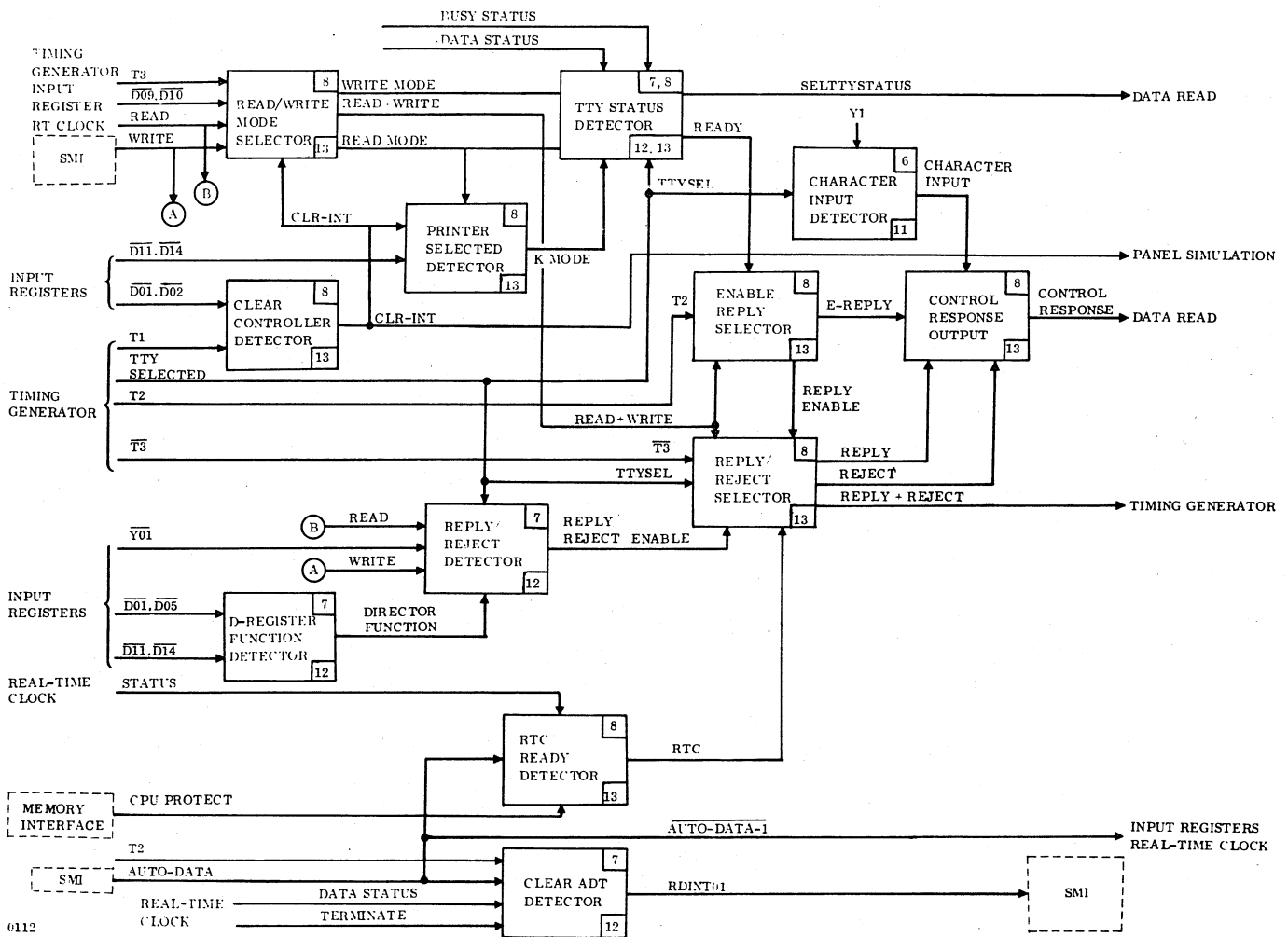


Figure 4-10. I/O-TTY Response Control Function

### ADT Detection

The TTY ADT interrupt (TTY-ADT-INT) sends an interrupt to the SMI to increment the auto-data transfer micro-level sequences used by the I/O-TTY controller. After the operating function has selected ADT, the clear ADT detector (latch D4, OR gate A4, and AND gate E1) [latch A5, OR gate A6, and AND gate D3] monitors the ADT line and permits the ADT sequence each time the data status remains active and the terminate signal is inactive. If the ADT sequence has been completed, a TERMINATE active signal is present at time T2 to inhibit the RDINT01/ to the SMI and to initiate the end-of-operation status that is sent to the status/interrupt selection function.

Normally when the ADT sequence is in progress, the RDINT01/ signal is alternately high and low as the data status signal changes.

The ADT-SELECTED signal is developed at flip-flop (D4) [A5] when director function word bit D7 produces a high at pin 13. This high sends Q output pin 15 high when the clock input (determined by a WRITE Y1 present at time T3) goes high to produce ADT-SELECTED. This signal remains high until a clear interrupt is applied to flip-flop D4.

RDINT01/ goes low when the clock input (derived by AUTO-DATA and T2 being high at K4) and TERMINATE are high at flip-flop (K1) [C3]. This terminate condition is

applied to AND gate (E1) [D3] and AND/OR gate (G6) [E1, D1] to inhibit RDINT01 and initiate the end-of-operation when ADT-SELECTED goes high.

### RTC

When the real-time clock function has been activated, it senses that AUTO-DATA, CPU PROTECT, and RTC SEL are all active. These conditions enable the reply/reject selector to send the reply signal response to a CPU read or write if the protect conditions are met. If the protect conditions are not met, a reject signal is sent.

When the real-time clock has been selected (W=0, E=1, S=7), the low output at AND gate (F1) [J3] pin 8 sets flip-flop (E2) [H3]. The next time T3 is high at pin 11, the Q output is high. This high is applied to AND gate (F2) [G7]. If AUTO-DATA/ or CPU-PROT/ at pins 12 or 13 of OR gate (L9) [M5] is low, a protect high is applied to pin (2) [4] of AND/OR gate (G1) [H2]. Since the real-time clock has been selected, pin (3) [5] of (G1) [H2] is also high to drive pin 6 low. This low inhibits the reject signal output at pin (12) [1] of AND gate (F2) [G7] and may be inverted by (G4) [G3] to enable the reply signal at pin (8) [11]. If the protect condition does not exist, the AND/OR gate output at pin 6 is high. This high enables the reject signal and inhibits the reply signal outputs of AND gates (F2) [G7].

## Read/Write Selection

When a write or read request is present and the associated bit (D09 = select write mode, D10 = select read mode) is active, read/write mode selector (J2) [K3] produces the read or write mode condition at time T3. This condition combines with the ready conditions (printer connected, data, busy, and TTY selected) to send a READY signal to the enable reply selector. When the ready condition is present at time T2, the enable reply selector produces the  $\overline{E}$ -REPLY control response for the data read function and enables the reply/reject selector. If these conditions do not exist, the reject condition is produced.

When either  $\overline{D9}$  (write mode) or  $\overline{D10}$  (read mode) is high at OR gate (G2) [J2] pins 9 or 10, a high condition exists at pin 13 of AND gate (H2) [K2]. If  $\overline{D9}$  is high, this high also enables read/write flip-flop (J2) [K3]. If the (WRITE)(Y1) condition is high at time T3, the write output is selected; if (WRITE)(Y1) is low, the read output is selected. The selected condition is ANDed with READ, WRITE, and Y1 at AND gate (D1) [G1]. The correct output is coupled through OR gate (C1) [F1] and ANDed with the data status condition. If DATA STATUS is high, the data status direction right ( $\overline{DS}$ )(DIR-RT) low output is applied to OR gate (G2) [J3]. This activates (G2)[J3], which enables flip-flop (E2) [H3]. At time T2, the (E2) [H3] flip-flop is set to provide the enable TTY reply signal ( $\overline{E}$ -REPLY) to OR gate (E1) [G1] and to initiate the read or write sequence at the UART.

## Character Input

The character input (CHAR INPUT) response is produced when TTYSEL and  $\overline{Y1}$  are high at pins (12 and 13) [1 and 2] of AND gate (D5) [C5]. (TTYSEL is high when AND gate (D7) [F7] detects that the Y register WES fields equal 0 1 1.) This drives the output (pin 11) [pin 3] of AND gate (D5) [C5] low, which is inverted by inverter (D6) [D4] and inversion AND gate (F2) [G7] to provide the CHARINPUT condition at pin (3) [6] of (F2) [G2]. This  $\overline{CHARINPUT}$  is coupled to the CPU via the data read logic (flip-flop J8 and multiplexer J7) [flip-flop G6 and multiplexer F6] to select the character data loading into the lower eight bits of the CPU A register.

## Director Functions

When the CPU requests a write operation, all functions that the TTY can perform will reply. The director function bits assigned to printer application (D11 = connect printer, D14 = disconnect printer) and the director function bits assigned for interrupt application (D01 = clear controller, D02 = clear interrupt, D03 = data interrupt request, D04 = end-of-operation interrupt request, and D05 = alarm interrupt request) are applied to the D register function detector. If one or more of these bits is active, a director function active condition is produced and combined with the write request to produce a reply enable. If none of these bits is active, the director function is inactive. This causes a reject enable.

## Reply/Reject

Since reply/reject flip-flop (E2) [H3] is latched during time T3, an enable is applied to reply/reject AND gates (F2) [G7]. D-register bits D01 through D05, D11, and D14 are applied to OR gates (C6, D2, and C5) [C6, B5, and B6]. If any of these bits is high, a low condition is applied to OR gate C6 pins (1 or 4) [5 or 4]. If pin 1, 2, 4, or 5 of OR gate C6 goes low, a high is applied to pin (2) [4] of AND gate (C1) [C5]. If this high is present at (C1) [C5] when (WRITE)(Y1) is high, (C1) [C5] applies a low to pin (5) [4] of OR gate (E1) [G1]. (E1) [G1] provides a high level ( $\overline{E}$ -TTYREPLY) to

AND/OR gate (G1) [H2] pin (5) [2]. If TTYSEL is also high, a low is applied to AND gate (F2) [G7] pin (12) [1], which inhibits the reject. This (G1) [H2] low condition is also applied to inverter (G4) [G3] to provide a high to AND gate (F2) [G7] pin (9) [12]. This activates (F2) [G7] to provide a reply low ( $\overline{REPLY}$ ) condition to the CPU via the data read function. If the director function bits are active but (WRITE)(Y1) is low (or vice versa), AND gate (C1) [C5] produces a high output that does not trigger OR gate (E1) [G1] but inhibits AND/OR gate (G1) [H2], which applies a high condition to the reject AND gate (F2) [G7]. (F2) [G7] sends REJECT to the CPU via the data read function. If READ and Y1 at pins (12 and 13) [1 and 2] of AND gate (C1) [C5] are both high, a low output from (C1) [C5] initiates a reply, providing TTYSEL is also high. If any of these signals is low, the reject is activated.

## Printer Selected (K Mode)

When data bits D11 or D14 are active at pins 12 or 13 of OR gate (C5) [B5], a high appears at AND gate (D2 pin 9) [K2 pins 1 and 2]. This high is ANDed with (WRITE)(Y1) and time T3. If all are high, a high is applied to the clock input of flip-flop (J2) [K2]. If data bit D11 is high (connect printer), data bit D14 is low. D14 low is applied to the enable input of (J2) [K3]. When the clock pulse is applied to (J2) [K3], the  $\overline{Q}$  output goes high and is ANDed with BUSYSTATUS at AND/OR gate (G1) [H2]. If both are high, the resulting output (low) is ANDed with (WRITE)(Y1) to produce a high output at AND gate (G2) [J2], which initiates a reject output and inhibits the  $\overline{E}$ -REPLY signal to the UART enable logic. If D11 is high and BUSYSTATUS is not active, the resulting output is AND/OR gate (G1) [H2] is high. This high is ANDed with the (WRITE)(Y1) high at AND gate (G2) [J2]. If both are input high at AND gate (G2) [J2], the reply signals are initiated.

## Clear Interrupt

The clear interrupt provides the clear controller signal to printer-connected (K MODE) and UART logic. This function is initiated when the WRITE and Y1 signals at Pins 4 and 5 of AND gate (C2) [B5] are high. (WRITE)(Y1) high output is applied to AND gate (C2) [K4] at time T1, pin (11) [8] of (C2) [K4] goes high. This high is applied to pins (9 and 5) [1 and 5] of AND/OR gate (H1) [K5] to generate the clear controller (CLR-CONT) and clear interrupt (CLR-INT) signals. If D1 is high at gate (H1 pin 10) [K5 pin 13], the clear controller output at pin 8 is applied to flip-flops (J2) [K3] to clear the printer-connected (K MODE) and UART logic. If D2 is high at (H1) [K5] pin 4, CLR-INT is applied to the ADT-selected, terminate, and manual interrupt logic.

## PANEL SIMULATION FUNCTION

The panel simulation function (figure 4-11) is available when associated firmware is supplied. It provides a modified panel mode capability when the breakpoint controller is not supplied. When the micro processor is operating as a CDC 1700 enhanced computer, the panel simulation function lets the operator control and display all registers and memory that may be used at the macro level. The control conditions provided by the simulated breakpoint controller function are external stop, selective stop, protect, selective skip, enable micro memory write, and multilevel indirect addressing. These conditions are under control of the CDC 1700 enhanced program panel simulation firmware and are available to the CPU via data bits D04 through D06 and D13 through D16. (The bit assignments are listed in table 4-3.) There are two panel simulation interrupts: RDINT12 advises the CPU that data is present and RDINT13 advises the CPU to send data to the UART.

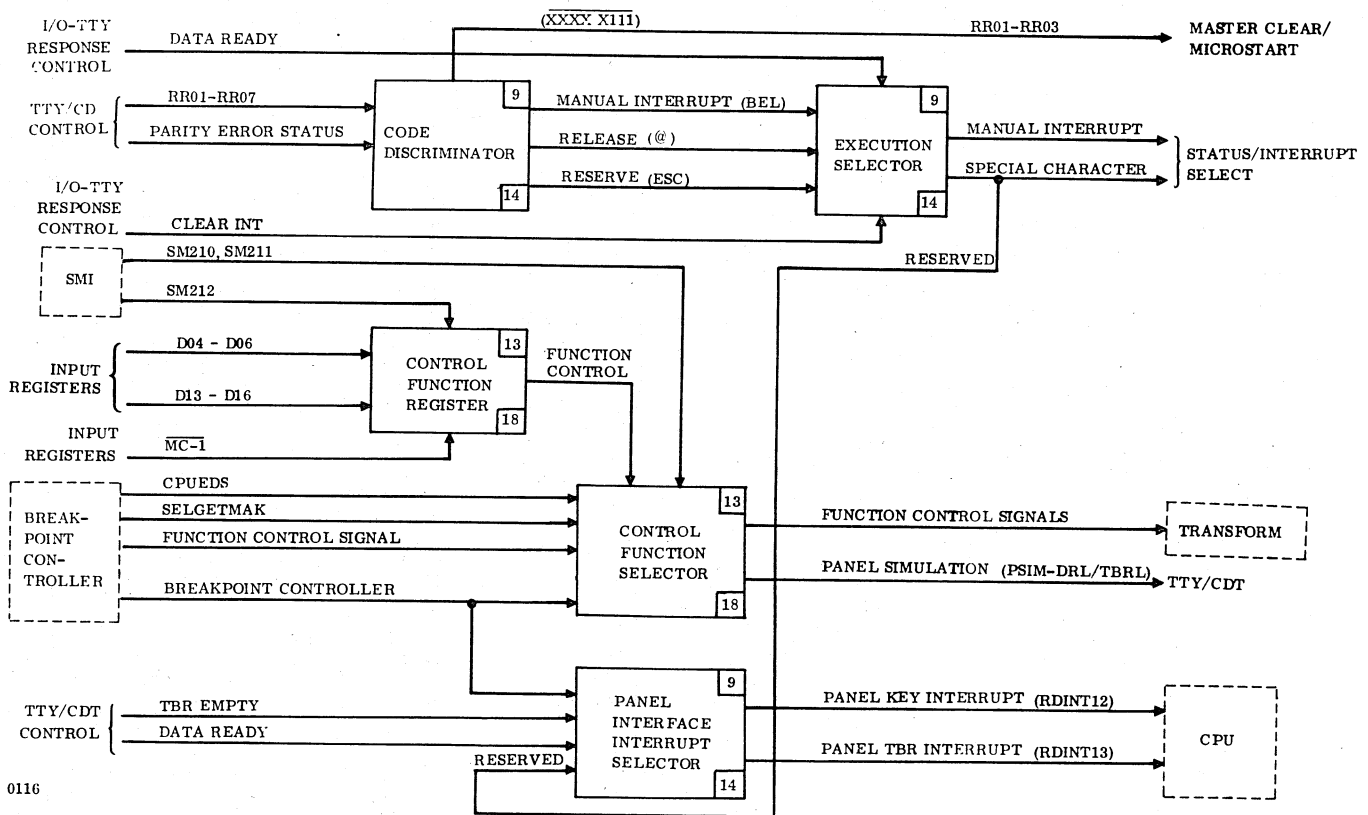


Figure 4-11. Panel Simulation Function

TABLE 4-3. FUNCTION CONTROL BIT DEFINITIONS

Bit	Definition
D04	Enable console echo
D05	Enable micro memory write
D06	Multilevel indirect addressing
D13	External stop
D14	Selective stop
D15	Selective skip
D16	Protect

When the breakpoint controller is supplied, resistor R10 maintains a high condition at the inputs of AND gates (K8 and L4) [G2] and inverter (M4) [G3]. These highs enable the RDINT12/ and RDINT13/ control functions controlled by AND gates (K8 and L4) [G2] and cause a low at the output of inverter (M4) [G3]. With the enable input and set inputs of multiplexers B10 and (H10) [H9] low, the outputs of panel simulation function control register flip-flops (C10 and G10) [B9 and G9] are enabled. Therefore, when data bits D04 through D06 and D13 through D16 contain a control function selection at the next high condition of SM212, the designated function is sent to the CPU. This is true for all except the EXSTOP function; before EXSTOP can be enabled by a high at pin (5) [12] of AND gate K10, the CPU-EDS/ and SELGETMAK/ signals applied to the inputs of AND gate J9 must be low to produce a high to pin (4) [13] of K10. If a master clear low (MC-1) is applied to the clear input of flip-flops (C10 and G10) [B9 and G9], all outputs are set low no matter what state exists on the CP and D inputs.

### Panel Simulation

When a breakpoint controller is supplied, a low (PNLPRES/) applied to inverter (M4) [G3] and AND gates (K8 and L4) [G2] inhibits the RDINT12/ and RDINT13/ AND gates. The output of inverter (M4) [G3] applies a high to (M3 pin 9) [F2 pin 12] to enable the application of a RESERVED signal (panel simulation active) to the I/O-TTY data ready logic and to the set inputs of 10-to-4-line multiplexers B10 and (H10) [H9], which enables the panel interface inputs (I1) and inhibits the simulation inputs (I0). This enabled condition inhibits the panel simulation (PSIM-DRR and PSIM-TBRL) signals by holding the B10, I1C, and I1D inputs at ground. A ground is also applied to I1A of (H10) [H9] to disenable AND gate K10 to inhibit selection of the EXSTOP/ control function.

### Special Character Code

The special character codes ESC, @, and BEL select the reserved status (I/O-TTY controller character data inactive, breakpoint controller character data active), release reserved status (I/O-TTY controller character data active, breakpoint controller character data inactive), and manual interrupt, respectively. Function and status operations within the I/O-TTY controller are still permitted. These character codes: ESC (1B<sub>16</sub>), @ (40<sub>16</sub>), and BEL (07<sub>16</sub>) are derived from data bits RR01 through RR07 applied to code discriminator multiplexers (K3 and L2) [E4 and F4]. (K3) [F4] detects the status of RR01 through RR03 and (L2) [E4] detects the status of RR04 through RR07 to initiate the selected action. The Q3 output of multiplexer (K3) [F4] pin

4 is low when RR01 through RR03 are all high (XXXX X111) and the Q0 output of (L2) [E4] pin 9 is low when RR04 through RR07 are all low (0000 0xxx). Adding these data bits produces binary code 0000 0111, which equals the BEL code (07<sub>16</sub>). Lows applied to pins (5 and 6) [8 and 9] of AND gate (L3) [F3] produce the high output (manual interrupt) applied to the manual interrupt detector logic of the status/interrupt function and inhibit the data ready response to the UART. The inhibit is produced when inverter (M4) [G3] provides a low to OR gate (L4) [G2], which produces a high at AND gate (M3) [F2] to inhibit the TTY data register ready (TTY-DRR) signal.

All special character codes are produced in the manner described above. Therefore, when both inputs at pins (2 and 3) [8 and 9] of AND gate (L3) [E3] are low (application of ESC code to (K3) [F4] and (L2) [E4]), a high is applied to OR gate (M2 pin 12) [F3 pin 5] and AND gate (M3) [F2] pin 2. This high produces a low at (M2 pin 13) [F3 pin 4], and since the @ symbol code has not been selected, a low exists at pin 2 of AND gate (M2) [F3]. These two low inputs at (M2) [F3] produce a high at pin 1 of (M2) [F3], which applies a high to pin 12 (D) of flip-flop (M1) [E2]. Since the flip-flop Q output is high, the high and low inputs at pins (5 and 6 of M2) [2 and 3 of E3] apply a low to pin 2 (D) of flip-flop (M1) [E2] (select the not released signal RELEASED) [deselect the release signal].

In addition, since data ready (DRDY) is high (indicating the presence of data, the escape code), the inverted output of M4 places a high at pin 1 of AND gate M3. The two high levels at pins 1 and 2 of M3 provide a low to set input pin 10 of flip-flop M1. With the low and high levels of pin 10 applied to pins 12 and 11 of M1, the Q output pin 9 becomes high to select the reserved status. [If data ready (DRDY) and escape (ESC) are both high at AND gate F2, a high-to-low transition is applied to one-shot MV L4. If the deadstart signal SM204 is high, this low applied to L4 will activate the one-shot MV. The SET-RSRV output goes high and sets reserve flip-flop E2 to provide an active condition for the breakpoint controller. When the output of AND gate F2 is high; if the SM204 input goes low, the one-shot MV is activated. This also causes the reserve flip-flop to be set.] RESERVED is coupled through the data read function to the CPU three-state bus. The high output at AND gate (L3 pin 1) [E3 pin 10] is also inverted by (M4) [G3] to apply a low at pin (3) [2] of OR gate (L4) [G2]. (L4) [G2] applies a high to pin (12) [9] of AND gate (M3) [F2] and a low to AND gate (K4 pin 9) [B3 pin 10]. Since the data ready signal at (M3 pin 12) [F2 pin 9] is low, the special character code is inhibited from entering the data receive register of the UART.

When the @ symbol code is selected by the TTY/CD, input pins (8 and 9) [11 and 12] of AND gate (L3) [E3] are low, driving pin (10) [13] high. Since the reserved condition is holding pin (11 of M2) [6 of F3] high, the low at pin (13) [4] being ANDed with the high from (L3 pin 10) [E3 pin 13] at AND gate (M2) [F3] produces a low-level output at (M2) [F3] pin 1. This low is applied to pin 12 (D input) of flip-flop (M1) [E2] to send the Q (pin 9) input low to remove the reserved status; at the same time, the low at AND gate (M2 pin 5) [E3 pin 3] is being ANDed with the low Q (pin 8) output of (M1) [E2]. These two low levels at (M2) [E3] produce a high that is applied to the D input of (M1) [E2], setting the Q (pin 5) output high to select the released status. In this case, the special character code is not inhibited from the UART and the @ symbol appears on the output display.

## TELETYPEWRITER/CD CONTROL FUNCTION

The teletypewriter/CD control function (figure 4-12) provides the I/O-TTY controller communication link for the transfer of character code data (teletypewriter, RS232-C,

or TTL level) to and from the CPU. The communication link provides three transmission interface methods:

- Teletypewriter (20 mA current loop)
- CD or breakpoint controller (RS232-C level)
- M05 or breakpoint controller (TTL level)

All external character codes are transmitted in asynchronous serial format, with a program-selectable data format of seven or eight bits with or without parity; parity is always even when selected. Each character data word format consists of a start bit, seven or eight data bits, a parity bit (if selected), and one or two stop bits (two stop bits when 110 baud is selected). All character data transferred within the CPU and I/O-TTY controller is parallel format of seven- or eight-character code bits.

This function also provides character echo response and sharing of the teletypewriter or CD between the I/O-TTY controller during program mode, and the panel interface controller during panel mode. This sharing is accomplished by processing particular special character codes (ESC, @, and BEL) as control characters. These codes are reserved as control codes and cannot be accepted as message data.

- Reserve status - The ESC (1B<sub>16</sub>) code transfers control of the TTY/CD from the I/O-TTY controller to the breakpoint controller.
- Release reserve - The @ (40<sub>16</sub>) code transfers control of the TTY/CD from the breakpoint controller to the I/O-TTY controller.
- Manual interrupt - The BEL (07<sub>16</sub>) code can be used to impose a manual interrupt from the input device rather than from a console manual interrupt switch.

The Y-register status field bits Y05, Y06, Y07, and (W=0)(EQ=1) are deciphered to detect the TTY selected (TTYSEL) condition. TTYSEL is combined with data bit D01 and (WRITE)(Y1) to produce the master reset that activates the UART master reset. The UART is cleared to permit loading of character code words into the UART receive register. Character code words are loaded at the rate of one bit for every 16 clock pulses. TTYSEL high is ANDed with function word bit D01 (clear controller) and (WRITE)(Y1). If all are high at AND gate (A2) [D3], a master reset condition appears at pin (8) [6]. Since a master clear is not in effect, MC-1 is high and the master reset condition produced by (A2) [D3] is present at OR gate (B1) [C5], the high is applied to the MR input of the UART. The UART logic resets to facilitate loading of data into the UART. At the same time, TTY DATA (a combination of TTYSEL and Y1) is inverted at (D6) [D4] and compared with the REPLY+REJECT, READ+WRITE, and E-REPLY signal at AND gate (B2) [H5]. If all are high, the result is compared with write mode (WT-MODE) at AND gate (F1) [B2] and with READMODE at AND gate (G2) [B2]. If WT-MODE is high, the transmitter loading is enabled; if READMODE is high, the receiver loading is enabled.

## Receiver Enabled

The receiver may be loaded from the teletypewriter, CD, any TTL serial data generator, or any device that produces a compatible RS232-C signal. The teletypewriter transmission line is a 20 mA current loop that is detected by 20 MA-to-TTL converter (Q2) [Q1] (see 20 mA-to-Digital Converter below). The RS232 inputs are ±3 to ±12 V amplitude signals that are converted to 0 to +5 V amplitude signals by converters (H5) [H6]. If any one of the four inputs

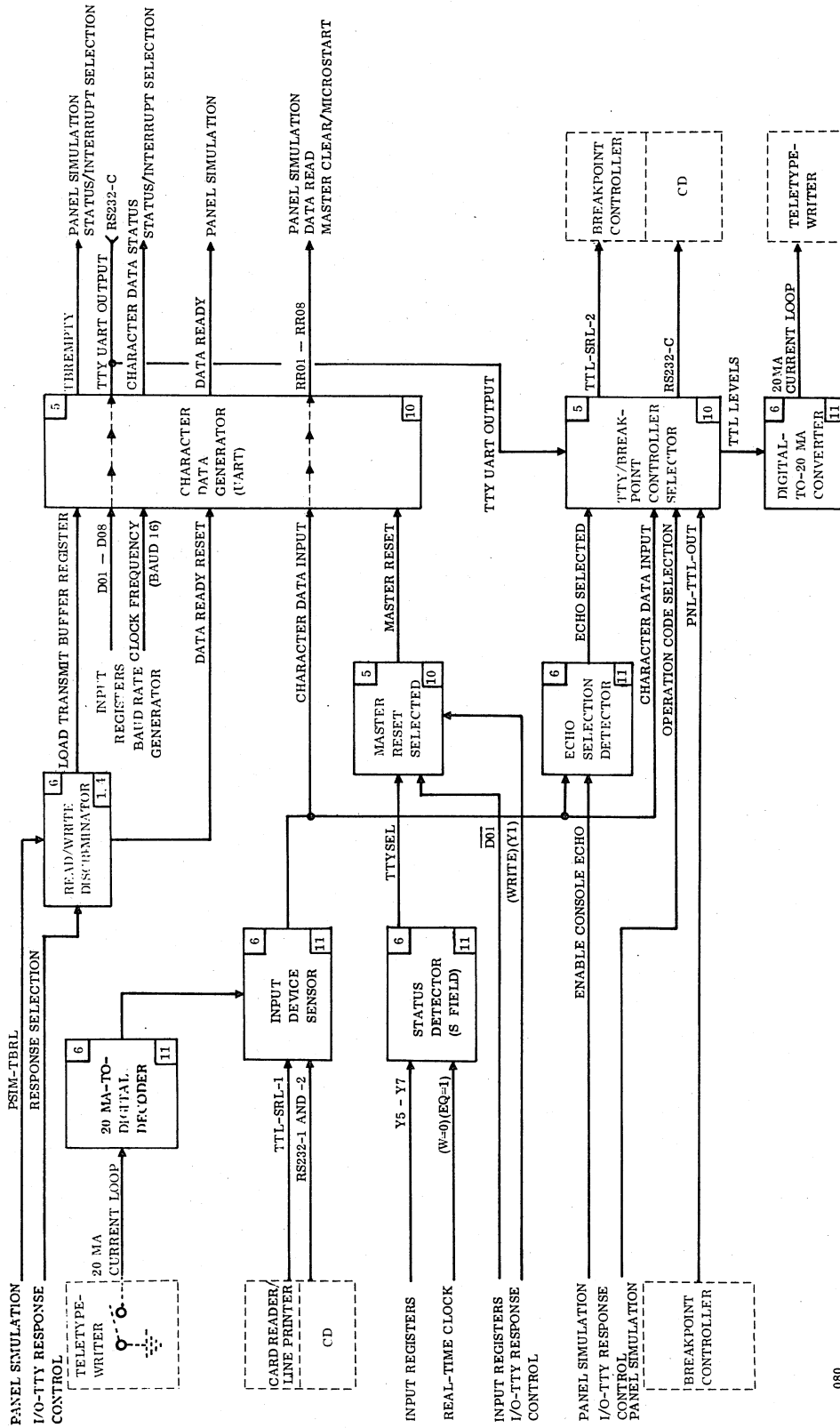


Figure 4-12. Teletypewriter/Console Display Control Function

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is active at OR gate (H2) [H5], the loading of the UART receiver register is enabled and the data codes are applied to selector multiplexer (E7) [E9]. The input data loaded into the UART (EF6) [DE6] receiver register is in asynchronous serial format; it has one start bit, seven data bits, one parity bit, and one or two stop bits. Data bits loaded into the receiver register are clocked in by the baud rate frequency generator (figure 4-17) at the rate of one bit every 16 Hz. When the receiver register is loaded and checked for parity, framing, and data status, a data ready signal is generated and the data is shifted to the receiver buffer register and held until a CPU read is generated.

The output data is transferred to the data read function (figure 4-14), master clear/microstart function (figure 4-16), and panel simulation function (figure 4-11). The parity error (P.E.), framing error (FERROR), and LOST DATA STATUS signals are sent to the status/interrupt function (figure 4-14). The data ready signal (DRDY) is sent to the panel simulation function and to AND gate (M3) [F2], where it is ANDed with the restricted codes (BEL, ESC, and @). If the restricted code signal is high, the AND gate low output is coupled through OR gate (H4) [D2] and (F8) [D2] to cause an immediate low at the UART DRR input. This low resets the UART data ready circuit to inhibit the data ready signal to the CPU.

The TTY/panel selector is a 7-to-1 multiplexer (E7) [E9], which selects the CD UART output, character data input, or the breakpoint controller with or without echo response in accordance with the operation code selection signals (breakpoint controller present, reserved, and printed connected). Refer to table 4-4. These signals are applied to selector inputs S0, S1, and S2 to select the output termination to either TTY, RS232-C, or TTL transmission line.

Transmission line compatibility is provided for the TTY, RS232-C, and TTL communication capabilities. The teletypewriter input and output signals are accomplished via a 20 mA current loop that must be converted to TTL levels for processing within the I/O-TTY controller. Input signals are converted from 20 mA current fluctuations by associated transistor circuits. The RS232-C input signals are converted from the RS232 signal levels (+3 to +12 volts to -3 to -12 volts) to TTL levels (0 to +5 volts) by the RS232 input converter. The RS232 output signals are converted from TTL level to the RS232-C level by a TTL-to-RS232 converter. Since the I/O-TTY controller is compatible with TTL inputs and outputs, the TTL serial and breakpoint controller lines do not require additional circuit elements.

Character data words to be transmitted during a CPU write command are loaded in parallel format into the transmit buffer register from the D register (see figure 4-7) via lines D1 through D8. This load transmit buffer register (TBRL) command is derived from response selection (write mode, E-REPLY, write, reply, and TTY DATA signals) and panel simulation (PSIM-TBRL) signals by the read/write discriminator. When either the response selection signal or panel simulation signal is true, the D-register data is loaded into the transmit buffer register. When the transmit buffer register is filled, the data is immediately transferred to the transmit register. As the word is transmitted, start, parity, and stop bits are added to the data word under control of the UART's word length control logic. This data word is transmitted in serial format to the CPU and respective control device at the rate of one bit for every 16 clock pulses. When the transmit buffer register is empty, a TB register empty signal (TBREEMPTY) is sent to the CPU via the status/interrupt selection function, indicating that a new word may be injected. When the transmit and transmit buffer registers are full, a busy signal is sent to the CPU via the status/interrupt selection function.

### 20 mA-to-Digital Converter

The 20 mA-to-digital converter (Q2) [Q1] is normally conducting due to the positive potential applied to the base. The positive potential is developed by the current flow through (R13, CR1, R14, and R15) [R3, CR1, R7, and R9] when the teletypewriter switch is open. When the teletypewriter switch is closed, ground is applied and current flows through (R13) [R3] to ground, causing the base to become less positive to backward-bias (Q2) [Q1] to cutoff. This cutoff condition of (Q2) [Q1] places approximately +5 volts at the collector to produce the high digital level. When the base voltage rises to forward-bias (Q2) [Q1] on the collector, voltage falls toward ground (approximately 0.6 volt) to produce the low digital level.

### Digital-to-20-mA Converter

The digital-to-20 mA converter (Q1) [Q2] is normally backward-biased by the +5 volts applied to the base that holds (Q1) [Q2] cutoff. This inhibits the current path to the teletypewriter. When the digital output at  $\bar{Q}$  of multiplexer (H6) [H4] goes low, current flow through (R20 and R21) [R8 and R10] forward-biases (Q1) [Q2] into conduction. This causes current flow from the teletypewriter through Q1 to +5 volts.

TABLE 4-4. I/O-TTY, BREAKPOINT CONTROLLER, ECHO SELECTION

Selection	PNLPRES (S2)	RESERVED (S1)	KMODE•RMODE (S0)	Selected Output
I/O-TTY	0	0	0	TTY UART-OUT echo†
	0	0	1	
Panel simulation	0	1	0	UART-IN PSIM-echo (simulated console echo)
	0	1	1	
TTY-breakpoint controller shared display	1	0	0	TTY UART-OUT echo
	1	0	1	
	1	1	0	Panel Interface Out (PNL-TTL-OUT)
	1	1	0	

† Echo - The ability to have the selected input character immediately displayed on the teletypewriter or CD.

## UART Description

The general-purpose, programmable, universal asynchronous receiver/transmitter (UART) has three-state outputs: 0, 1, and hi-Z. It is TTL-compatible (refer to figure 4-6). It is capable of simultaneously converting asynchronous serial binary characters to a parallel format (receiver) and parallel characters to serial, asynchronous output (transmitter) with start, parity, and stop bits added or verified. The programmable features are word length, information rate, parity, parity inhibit, and stop bit generation (refer to figure 4-13 and table 4-5).

## STATUS/INTERRUPT SELECTION FUNCTION

The status/interrupt selection function (see figure 4-14) provides I/O-TTY controller status data to the CPU via the data read function and macro interrupts to the SMI.

Character data status signals (parity error, lost data, and framing error) are received from the UART error detector logic. They are combined with a ready status signal from the CPU in the character data failure detector logic to produce the character data failure status that is coupled to the TTY status discriminator. If a failure status exists, the particular status is coupled via the data read function to the CPU. P.E., FERROR, and LOST DATA STATUS are inverted by (E5) [D4] and applied to OR gate (E4) [C6]. If any one of the conditions exists at the UART, (E4) [C6] produces a high indicating to the CPU that an alarm status exists. The lost data and ready status highs are applied directly to the data output multiplexer and the parity error status high is inverted by (F5) [D5] before it is coupled to data output multiplexer.

The character data status from the UART is also coupled to the data status detector and combined with the special

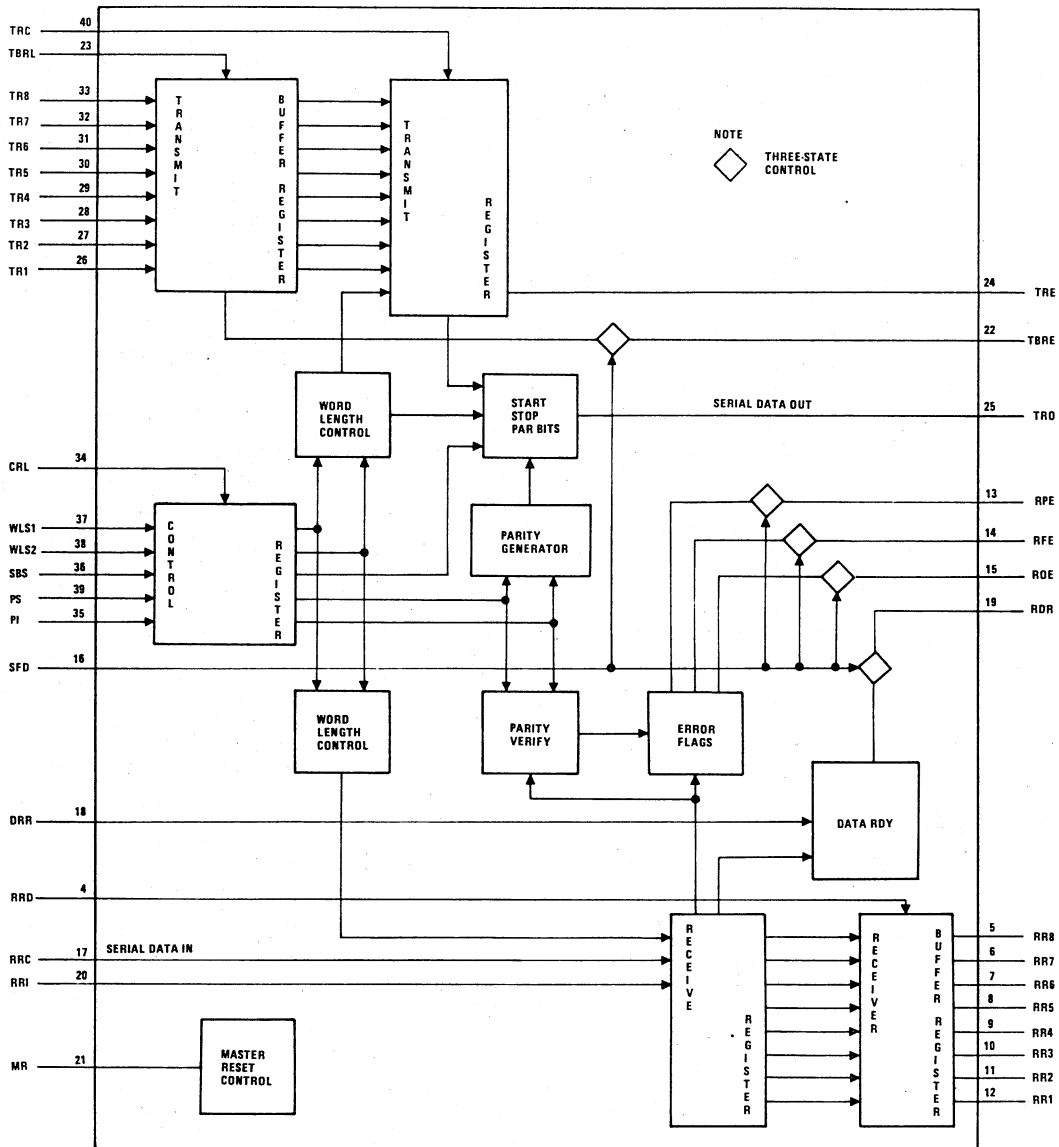


Figure 4-13. UART Functional Block Diagram

TABLE 4-5. UART PIN DESIGNATIONS AND DESCRIPTIONS

Designation	Pin No.	Description	Function
RRB (RBRD)	4	Receiver register disconnect	A high-level input voltage, $V_{IH}$ , applied to this line disconnects the receiver holding register outputs from the RR8-RR1 data outputs (pins 5 through 12).
RR8-RR1	5 through 12	Receiver buffer (holding) register data	The parallel contents of the receiver register appear on these lines if a low-level input voltage, $V_{IL}$ , is applied to RRD. For character formats of fewer than eight bits received characters are right-justified (RR1 = LSB) and the truncated bits are forced to a low output voltage $V_{OL}$ .
RPE	13	Parity error	A high-level output voltage, $V_{OH}$ , on this line indicates that the received parity does not compare to that programmed by the even parity enable (PS) control line (pin 39). This output is updated each time a character is transferred to the receiver buffer register. RPE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the status flag disconnect (SFD) line (pin 16).
RFE	14	Framing error	A high-level output voltage, $V_{OH}$ , on this line indicates that the received character has no valid stop bit; that is, the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the receiver holding register. RFE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the status flag disconnect (SFD) line (pin 16).
ROE	15	Overrun error	A high-level output voltage, $V_{OH}$ , on this line indicates that the data received flag RDR (pin 19) was not reset before the next character was transferred to the receiver holding register. ROE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the status flag disconnect (SFD) line (pin 16).
SFD	16	Status flag disconnect	A high-level input voltage, $V_{IH}$ , applied to this pin disconnects RPE, RFE, ROE, RDR, and TBRE, allowing them to be bus-connected.
RRC	17	Receiver register	The receiver clock frequency is 16 times the desired receiver shift rate.
DRR	18	Data received reset	A low-level input voltage, $V_{IL}$ , applied to this line resets the DRR line.
RDR	19	Data ready	A high-level output voltage, $V_{OH}$ , indicates that an entire character has been received and transferred to the receiver holding register.
RRI	20	Receiver input	Serial input data received on this line enters the receiver register at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, $V_{IH}$ , must be present when data is not being received.
MR	21	Master reset	This line is strobed to a high-level input voltage, $V_{IH}$ , to clear the logic. It resets the transmitter and receiver registers, the receiver holding register, RFE, ROE, RPE, and DRR, and sets the serial output line to a high-level output voltage, $V_{OH}$ .
TBRE	22	Transmitter buffer register empty	A high-level output voltage, $V_{OH}$ , on this line indicates that the transmitter holding register has transferred its contents to the transmitter register and may be loaded with a new character.

TABLE 4-5. UART PIN DESIGNATIONS AND DESCRIPTIONS (Contd)

Designation	Pin No.	Description	Function															
TBRL	23	Transmitter buffer register load	A low-level input voltage, $V_{IL}$ , applied to this line enters a character into the transmitter holding register. A transition from a low-level input voltage, $V_{IL}$ , to a high-level input voltage, $V_{IH}$ , transfers the character into the transmitter register if the register is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until the transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.															
TRE	24	Transmitter register empty	A high-level output voltage, $V_{OH}$ , on this line indicates that the transmitter register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.															
TRO	25	Transmitter register output	The contents of the transmitter register (start bit, data bits, parity bit, and stop bit) are serially shifted out on this line. When no data is being transmitted, this line remains at a high-level output voltage, $V_{OH}$ . Start of transmission is defined as the transition of the start bit from a high-level output voltage, $V_{OH}$ , to a low-level output voltage, $V_{OL}$ .															
TR1-TR8	26 through 33	Transmitter register, data inputs	The character to be transmitted is loaded into the transmitter holding register on these lines with the TBRL strobe. If a character of less than 8 bits has been selected (by WLS1 and WLS2), the character is right-justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, $V_{IH}$ , causes a transmission of a high-level output voltage, $V_{OH}$ .															
CRL	34	Control register load	A high-level input voltage, $V_{IH}$ , on this line loads the control register with the control bits (WLS1, WLS2, RPE PI, and SBS). This line may be strobed or hard-wired to a high-level input voltage, $V_{IH}$ .															
PI	35	Parity inhibit	A high-level input voltage, $V_{IH}$ , on this line inhibits the parity generation and verification circuits and clamps the RPE output (pin 13) to $V_{OL}$ . If parity is inhibited, the stop bit(s) immediately follows the last data bit on transmission.															
SBS	36	Stop bit(s) select	This line selects the number of stop bits to be transmitted after the parity bit. A high-level input voltage, $V_{IH}$ , on this line selects two stop bits; a low-level input voltage, $V_{IL}$ , selects a single stop bit. Selection of two stop bits when programming a 5-bit word generates 1.5 bits from the UART.															
WLS2-WLS1	37,38	Word length select	<p>These lines select the character length (exclusive of parity) as follows:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>WLS2</th> <th>WLS1</th> <th>Word Length</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>5 bits</td> </tr> <tr> <td>0</td> <td>1</td> <td>6 bits</td> </tr> <tr> <td>1</td> <td>0</td> <td>7 bits</td> </tr> <tr> <td>1</td> <td>1</td> <td>8 bits</td> </tr> </tbody> </table>	WLS2	WLS1	Word Length	0	0	5 bits	0	1	6 bits	1	0	7 bits	1	1	8 bits
WLS2	WLS1	Word Length																
0	0	5 bits																
0	1	6 bits																
1	0	7 bits																
1	1	8 bits																
PS	39	Parity select	This line determines whether even or odd parity is to be generated by the transmitter and checked by the receiver. A high-level input voltage, $V_{IH}$ , selects even parity; a low-level input voltage, $V_{IL}$ , selects odd parity.															
TRC	40	Transmitter register clock	The transmitter clock frequency is 16 times the desired transmitter shift rate.															

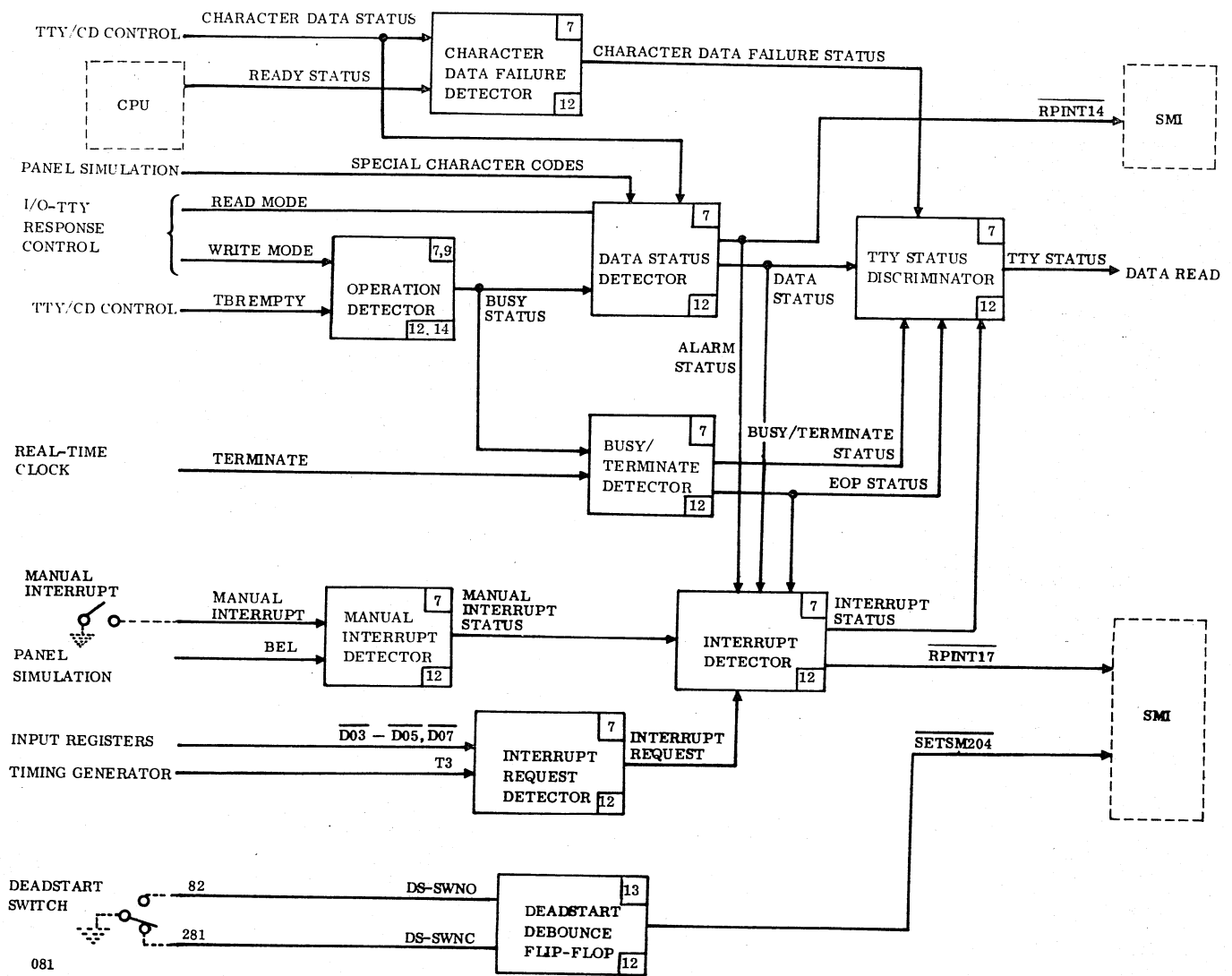


Figure 4-14. Status/Interrupt Selection Function

character codes (BEL, ESC, @), read mode, and the busy status output of the operation detector logic. This busy status is produced from write mode and UART register conditions. If the character data status contains a failure, the data status detector produces an interrupt (INT14) to the SMI and inhibits the data status output. If no failures exist during read mode when a special character code is present, the special code data status is coupled to the CPU.

During write mode, if the transmit registers signal indicates that the registers are full, the operation detector produces a busy status. When registers are empty, BUSY STATUS is inhibited or, if a terminate signal is applied to the busy/terminate detector logic, an end-of-operation (EOP) status is sent to the CPU.

Data ready (DRDY) and the special character codes are ANDed by (K4) [B3]; if both are high, the high is ANDed with LOST DATA STATUS and READ MODE at AND gate (E4) [D1]. If all are high (indicating that data is ready, a special code has been selected, a lost data status does not exist, and read operation is selected) AND gate (E4) [D1] produces a low that is inverted by OR gate F1 to produce a DATA STATUS high to the CPU. If, during write mode (high), the transmit buffer register is empty (TBEMPTY high), AND gate (F1) [E1] provides a low to OR gate (F1)

[E1], which also provides a write data status to the CPU. When either TBEMPTY or TEMPTY is low, OR gate D1 provides a BUSY STATUS and EOP STATUS to the CPU. When either transmit register is empty, the output of OR gate D1 is high and is inverted by (G4) [A3] to provide EOP STATUS.

When the manual interrupt switch at the console is activated or special character code BEL is injected, the manual interrupt detector produces an associated signal. This manual interrupt status generates an interrupt (RPINT17) for the SMI and a manual interrupt status for the CPU. If any of the D03 through D05 and D07 data signals are present during time T3, the interrupt request detector sends an interrupt to the interrupt detector logic. If an alarm, data, or EOP signal is present during these conditions, interrupt RPINT17 is produced and an interrupt status is sent to the CPU.

Interrupt status and interrupt RPINT17 are developed from the data, EOP, alarm status, released, or manual interrupt conditions. When data bit D03, D04, or D05 is low, one or more of the (D4) [A5] flip-flops is set. When the clock pulse is present, the associated flip-flop is latched. If the data, EOP, or alarm status signal is high, an interrupt status and RPINT17 is produced.

Manual interrupt is accomplished by activating the manual interrupt switch at the console or selecting the BEL code at the input device keyboard. The switch activation sets and resets flip-flop (L1) [C2], which sends a strobe pulse through OR gate (L1) [C2] to flip-flop (K1) [C3]. Since the S and D inputs of (K1) [C3] are tied high, the strobe causes a manual interrupt to be produced by INT17. If the BEL key initiates the manual interrupt cycle, AND gate (M3) [F2] initiates the manual interrupt in the same manner as switch flip-flop (L1) [C2].

A deadstart interrupt (SETSM204) can also be produced by the I/O-TTY controller. If the deadstart switch is activated, the debounce flip-flop is activated for one cycle. This produces a single positive pulse output to apply a clear SET SM204 high level to the SMI without sensitivity to the transient pulses generated by the switch.

When the deadstart switch is activated, flip-flop (L11) [M5] is set and reset. The flip-flop output is inverted by (K11) [E7] to produce a SET SM204/ low.

### DATA READ FUNCTION

The data read function (see figure 4-15) provides for the transfer of I/O controller data (character data, TTY/CD status, RTC status, RTC status, I/O control responses, and I/O data RD01 through RD16) to the CPU three-state bus. The data

to be gated onto the three-state bus is determined by a combination of the contents in the micro instruction B' field and the Y register at the time the micro instruction is executed. The Y register selection is decoded in accordance with the CDC 1700 WES/D convention when the micro instruction B1 field equals 010 (2<sub>0</sub>) to designate INRD (input data/status from I/O channel). Which data is selected for transfer to the CPU three-state bus is indicated in table 4-6. The I/O control response selection is determined when micro instruction B' equals 011 (3<sub>0</sub>) to designate INRS (input to S2 I/O response signal) (refer to table 4-7).

TABLE 4-6. Y REGISTER SELECTION OF READ DATA

W	E	S	D	Data Gated to CPU Three-State Bus
0	1	1	0	TTY/CD data
0	1	1	1	TTY/CD status
0	1	7	-	Real-time clock status
-	-	-	-	Data from peripheral controllers (RD01 through RD16)

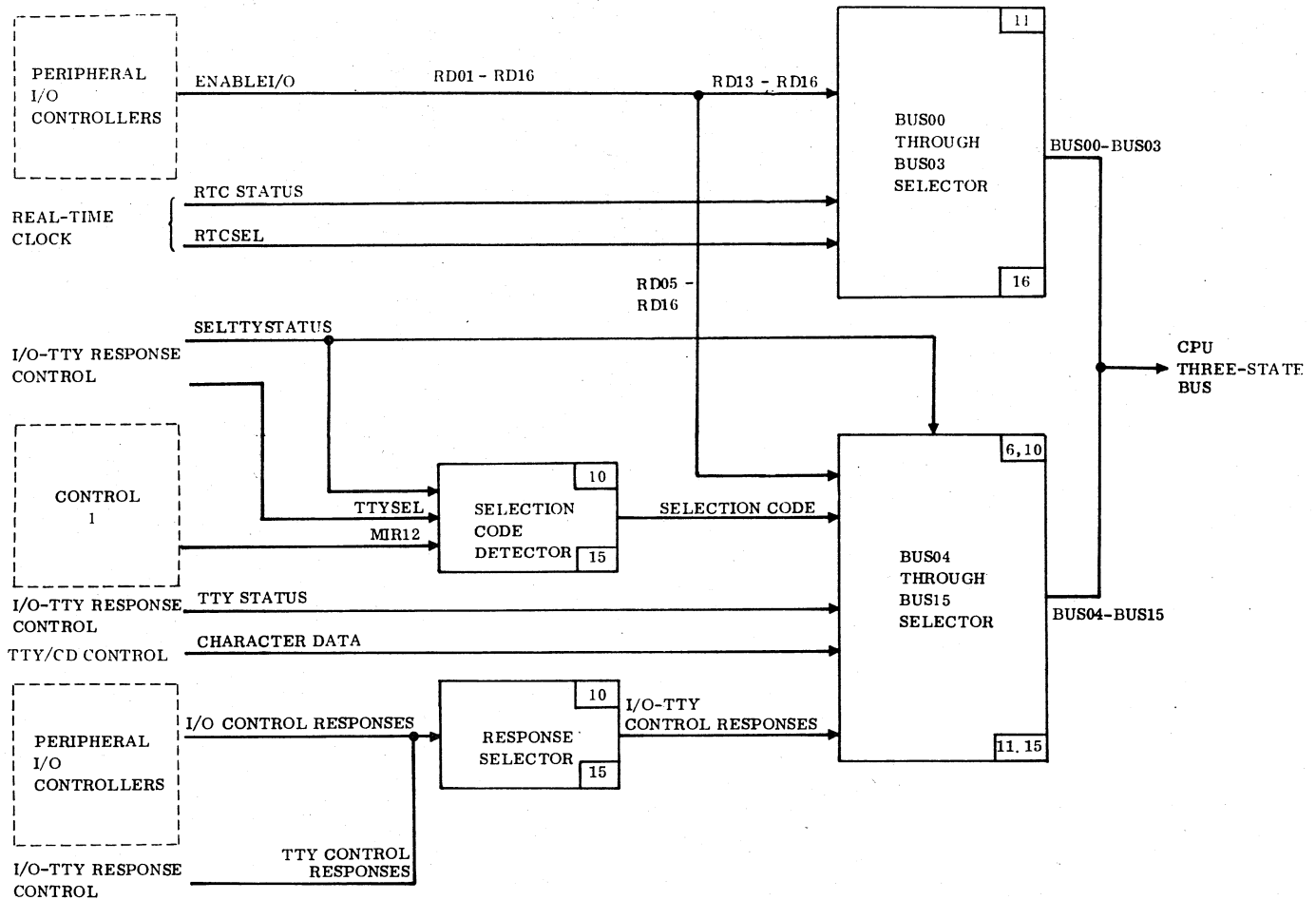


Figure 4-15. Data Read Function

TABLE 4-7. MICRO INSTRUCTION B' FIELD SELECTION

M05 Peripheral	CDC 1700 Peripheral	Three-State Bus Bit Position
Undefined	Undefined	00 and 01
Position 00	Receiver terminate (R-TERM)	02
Position 01	Reply	03
Position 02	Reject	04
Direction	Character input	05
Undefined	Undefined	06 through 15

This selection is performed by two 2-to-1 multiplexers, (E7 and H7) [E9 and E8], and four 4-to-1 multiplexers (A7, B7, J7, and K7) [F6, G5, C7, and A7]. The 2-to-1 multiplexers effect selection by the signals applied to the S and E inputs, and the 4-to-1 multiplexers effect the selection by decoding the S0 and S1 input conditions when the enable signal is low (refer to table 4-8). All data is received from the peripheral controllers via open collector lines RD01 through RD16 applied to the associated (C7, E8, and G7) [A8, B8, C8, D8, and D9] inverters.

TABLE 4-8. BUS08 THROUGH BUS15 SELECTOR SELECTION

S1	S0	Data Transferred to CPU Three-State Bus
0	0	I/O data (RD01 through RD08)
0	1	TTY/CD status
1	0	Character data (RR01 through RR08)
1	1	I/O-TTY control responses

Selector multiplexer (H7) [E8] provides the selection of RTC status and peripheral data lines RD13 through RD16. When RTCSEL is high (refer to table 4-6) and the ENABLEIO signal is low, the RTC limit and LOST COUNT STATUS are transferred to three-state bus lines BUS00 and BUS01. When both RTCSEL and ENABLEIO are low, RD13 through RD16 are transferred to bus lines BUS00 through BUS03.

Selector multiplexer (E7) [E9] provides selection of TTY/CD status (MANINTSTATUS, RESERVED, RELEASED, and READMODE) and peripheral data lines RD09 through RD12. When SELTTYSTATUS is high and ENABLEIO is low, the TTY/CD status is transferred to three-state bus lines BUS04 through BUS07. When SELTTYSTATUS and ENABLEIO are low, RD09 through RD12 are transferred to bus lines BUS04 through BUS07.

Selector multiplexers (A7, B7, J7, and K7) [A7, C7, F6, and G5] provide selection of peripheral data lines RD01 through RD08, TTY/CD status and data, and I/O controller control responses. This selection is determined by the signals applied to the multiplexer S0 and S1 inputs (refer to table 4-8). When SELTTYSTATUS is low, (TTYSEL)(Y1) is high, and MIR12 is low, inverter (F7) [L6] provides lows to

OR gates (F7) [L6] that set S0 and S1 low. When ENABLEIO becomes low, the data on lines RD01 through RD08 is transferred to the bus lines. When SELTTY STATUS is high, (TTYSEL)(Y1) is high, and MIR12 is low, (F7 pin 11) [L6 pin 6] is low. This low is applied to OR gate (F7 pin 1) [L6 pin 9], which applies a high to S0 input. When ENABLEIO is low, the TTY controller status data at multiplexer inputs DA1 and EB1 is applied to the bus lines. When SELTTYSTATUS, (TTYSEL)(Y1), and MIR12 are all low, pin (6) [11] of OR gate (F7) [L6] is high, setting S1 of (B7) [C7] high. When ENABLEIO goes low, the TTY/CD character code data RR1 through RR8 is transferred to the bus lines. When MIR12 is high, SELTTYSTATUS is low, and (TTYSEL)(Y1) is high, the output at pin (8) [3] of inverter (F7) [L6] is low. This applies low to both (F7) [L6] OR gates, the outputs of which go high to apply highs to both the S0 and S1 inputs. When ENABLEIO is low, the I/O-TTY controller or other I/O controller control response is transferred to the bus lines.

The I/O-TTY controller and other I/O controller control responses (CHARINPUT, RTERM, REPLY, and REJECT) are all applied to the D-latch flip-flop, (J8) [G6]. If any one of these signals is high at input D, the flip-flop is latched. When the RESYNC-I/O signal applied to CP rises, the latching signal is transferred through the flip-flop to the output multiplexer. If S0 and S1 of the output multiplexer are high, the control response is transferred to the bus lines.

#### REAL-TIME CLOCK FUNCTION

The real-time clock pulses (figure 4-16) are processed in the CPU auto-data transfer routine to provide the CPU with a time-lapse capability that can be directly related to process program time segments or time of day (see table 4-9). This elapsed-time base is produced by a pulse generator that emits a pulse every 3.3 milliseconds. These pulses are coupled from the real-time clock via the data interrupt line (RDINT08) to increment the clock counter field every 3.3 milliseconds. When the clock counter field equals the limit interrupt (LIMITINT-STATUS), the micro instruction send terminate signal (STERM/) is generated by the SMI to enable program interrupt RPINT24/, which terminates the real-time clock sequence. If a lost count interrupt is detected, an STERM signal is also generated to enable an RPINT24 signal to terminate the real-time clock sequence. When the sequence has been terminated by either a limit or a lost count interrupt, an associated status signal (LIMITINSTSTATUS or LOSTCOUNTSTATUS) is produced to advise the CPU which condition terminated the real-time clock sequence.

The converter, equipment, and status detectors decipher the Y register address bits to determine whether or not the real-time clock function code (WES=0 1 7) exists. The converter (W) field condition bits, Y13 through Y16, are detected by AND gate (J10) [F2]. If all bits are ones, a high output is applied to AND/OR gate (G6) [H10]. This high is ANDed with Y12; if Y12 is high or AUTO-DATA at gate (G6) [H10] is high, the WE0 signal is generated. WE0 is inverted by (G7) [H8] and is coupled through pins (10) [8] and (11) [9] to all peripheral I/O controllers and AND gate (K4) [J8]. The equipment (E) field, bits Y08 through Y11, are then deciphered. The WE0 condition is ANDed with the least significant E-field bit, Y08, at AND gate K4. If Y8 and WE0 are high and Y9, Y10, and Y11 are high at AND gate (M5) [L8], the resultant (W=0)(EQ=1) condition is produced. The status (S) field, bits Y05 through Y07, are then deciphered. If Y5, Y6, and Y7 are high and (W=0)(EQ=1) is high at AND gate (D7) [C4], the RTCSEL, established by W=0, E=1, and S=7, is generated.



The high inputs (TERMINATE, Y1, and AUTO-DATA READ) produce a low output at AND gate (L5) [L9]. This low sets the limit status flip-flop, which initiates a RPINT24/ low signal. The CPU sends a WRITE signal to terminate the real-time clock sequence, and a limit status signal to the CPU. If, at any time during the real-time clock sequence, a master clear signal ( $\overline{MC-I}$ ) is applied to latch flip-flops (K5 and K6) [J9 and K9], the output produces a RPINT24/ condition that also terminates the real-time clock sequence.

The clock generator receives real-time clock strobe pulses from the baud rate generator. These pulses are the result of the crystal frequency 4.9152 MHz being divided by four in the baud rate generator to produce a pulse frequency of 1.2288 MHz. This frequency is divided by 64 by multiplier (L8) [M6] and the resultant 0.0192 MHz frequency is again divided by 64 by multiplier (L7) [M7]. The output of (L7) [M7] is 300 Hz (3.3-millisecond pulse train appearing at the CP inputs of the lost count and interrupt flip-flops). This pulse train is always present and is only permitted out when the real-time clock sequence has been selected. (Refer to figure 4-17 for the real-time clock timing sequence.)

### MASTER CLEAR/MICROSTART FUNCTION

The master clear/microstart function (figure 4-18) clears the I/O controllers and initiates the micro programs enable. The master clear operation can be initiated from several sources: the master clear switch, a TTY/CD question mark (?) or the application of an MC signal from control 1. The microstart is a function of the panel interface not being supplied as part of the computer and the MCDELAYED/ signal not being active. When the breakpoint controller is supplied, the breakpoint controller logic provides the microstart signal to the control 1 module. A master clear signal ( $\overline{MC-S}$ ) can be generated via the I/O-TTY controller only when the breakpoint controller is not supplied. In this case, an external momentary switch must be connected across the master clear input lines to the debounce flip-flop.

A micro program is normally activated by the breakpoint controller; when this controller is not supplied, micro programs are enabled when the I/O-TTY controller supplies a microstart low signal (MICROSTRT/) to the control 1 module. The MICROSTRT/ signal is produced by AND gate K10 when the breakpoint controller present line (PNLPRES) and the master clear delayed line (MCDELAYED/) are high. This causes a constant MICROSTRT signal (except during a master clear) when the breakpoint controller is not present.

A master clear start low signal ( $\overline{MC-S}$ ) initiates a master clear cycle.  $\overline{MC-S}$  is coupled to the control 1 module that, under control of the CPU, produces a master clear low (MCDELAYED/). This signal is inverted by (K2) [L5] to produce the MC signal used to clear the I/O control function. The MC signal is also inverted by additional (K2) [L5] inverters to produce the  $\overline{MC-I}$  and  $\overline{MR}$  signals. The  $\overline{MC-I}$  signal clears the timing generator, panel simulation, and real-time clock functions.  $\overline{MR}$  is coupled across backplane bus terminal 277 to clear all the I/O controllers.

The master clear switch circuit contains a debounce flip-flop to eliminate the switch transients. When the MC switch is activated, backplane terminal 282 goes low and 83 goes high. This causes a high output at the debounce flip-flop AND gate (L11) [L10] pin 8, which applies a high to OR gate (L11 pin 5) [L10 pin 4]. Highs at pins 4 and 5 of OR gate (L11) [L10] send the output at (L11) [L10] pin 6 low. This high-to-low transition activates one-shot (K9) [L4], which produces a high output at pin 6 for 5 microseconds and inhibits AND gate (L11) [L10] to render the AND insensitive to transient pulses. The one-shot output high and the

breakpoint panel present high at AND gate K10 produces an  $\overline{MC-S}$  signal at backplane terminal 74, which is coupled to the control 1 terminal 93.

If  $\overline{MC-S}$  is initiated by a question mark (?) code (UART outputs RR01 through RR08 =  $3F_{16}$ ), gates (J9 and H9) [E3 and C4] detect this character code. AND gate (J9) [E3] ANDs the  $RR0 \cdot RR1 \cdot RR2$  (XXXX X111) low signal (obtained from the panel simulation function) with RR7 low to produce a high at pin (9) [13] of AND gate (H9) [C4]. This high from (J9) [E3] is ANDed with the high state of RR4, RR5, and RR6 to determine the  $3F_{16}$  condition (? code). The ? selected (RR4-RR7) high state is produced by AND gate (H4) [D7]. This question mark selected  $\cdot$ RESERVED high condition is then ANDed with data ready (DRDY/) at AND gate (F8) [D2]. If both inputs (pins (12) [2] and (13) are true (high), the output of (F8) [D2] pin (11) [12] rises, triggering one-shot (K9) [L4], which applies a high to pin 2 of AND gate K10. This high at pin 2 and the high at pin 1 (determined by the absence of a breakpoint controller) effect an  $\overline{MC-S}$ / low condition at pin 3 of AND gate K10.  $\overline{MC-S}$ / low is coupled to the control 1 module to initiate a master clear cycle.

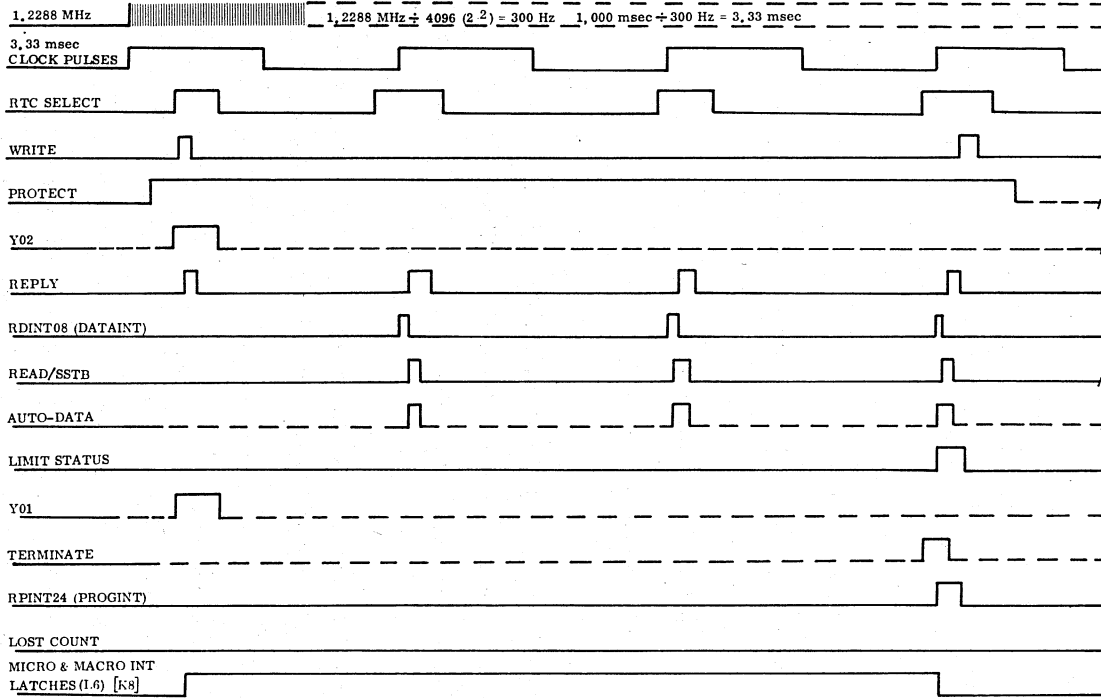
### BAUD RATE GENERATOR FUNCTION

The baud rate generator (figure 4-19) generates the UART clock frequencies required to operate at the four baud rates of 110, 300, 1200, and 9600. These clock frequencies are 16 times the baud rate (UART transmit and receive register shift rate). The various outputs provided by the baud rate generator are a high-level voltage to the UART stop bit select (SBS) input, the clock frequency for the transmit and receive registers (TRC and RRC), the complement of the clock frequency (DSUARTCLK) to the card reader/line printer controller UART, strobe frequency of 1.2288 MHz for the real-time clock, and selectable deadstart baud rates (PNLBAUD0 and PNLBAUD1) for the breakpoint controller. Switch (S1) [SW1] provides for selection of the clock frequencies associated with the controller baud rate requirements as indicated in table 4-10.

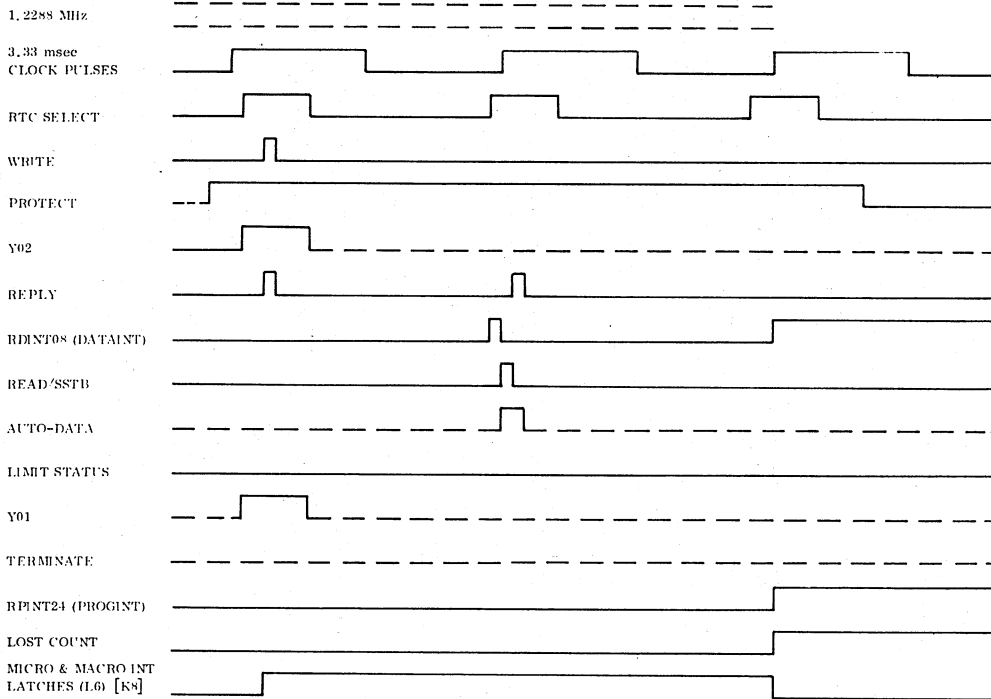
The baud rate generator receives a clock frequency of 4.9152 MHz from the crystal-controller oscillator located in the control 2 module of the CPU. This clock frequency is inverted by buffer (A4) [E1] and simultaneously applied to the clock pulse terminals of a 12-bit counter (A5, A6, and B5) [J7, K6, and K7] to produce the various baud rate clock frequencies required by the UART as well as the strobe frequency required by the real-time clock. Counter (A5) [K7] divides the 4.9152 MHz signal by 4 and 16. The divide-by-four output provides the real-time clock strobe frequency of 1.2288 MHz. The divide-by-16 output provides a 0.3072 MHz input to (A6) [K6] where the frequency is again divided by 32 and 256 to provide clock frequencies of 0.1536 MHz and 0.0192 MHz, respectively. The 0.1536 MHz signal is the clock frequency for 9600 baud rate ( $9600 \times 16$ ) and the 0.0192 MHz signal is the clock frequency for 1200 baud rate ( $1200 \times 16$ ). The 0.0192 MHz (TC) signal is coupled to counter (B5) [J7] to generate the clock frequencies for the 110 and 300 baud rates. Clock frequency 0.0048 MHz ( $300 \times 16$ ) is the direct result of the  $2^{10}$  output, but additional manipulation of signals is required to produce the  $110 \times 16$  clock frequency.

High outputs Q0 and Q1 of counter (B5) [J7] are ANDed by (C5) [J8], and the (B5) [J7] low output is inverted by (D6) [H8]. When these outputs are high and coincident with highs from TC of (A6) [K6] and QA of selector (B6) [J6] and AND gate (C6) [H7], a low output is produced by (C6) [H7]. It presets all the counters (A5, A6, and B5) [J7, K6, and K7], thereby advancing the output frequency at Q3 of (B5) [J7] by approximately 570 Hz to produce the clock frequency of

NORMAL RTC SEQUENCE



LOST COUNT CONDITION

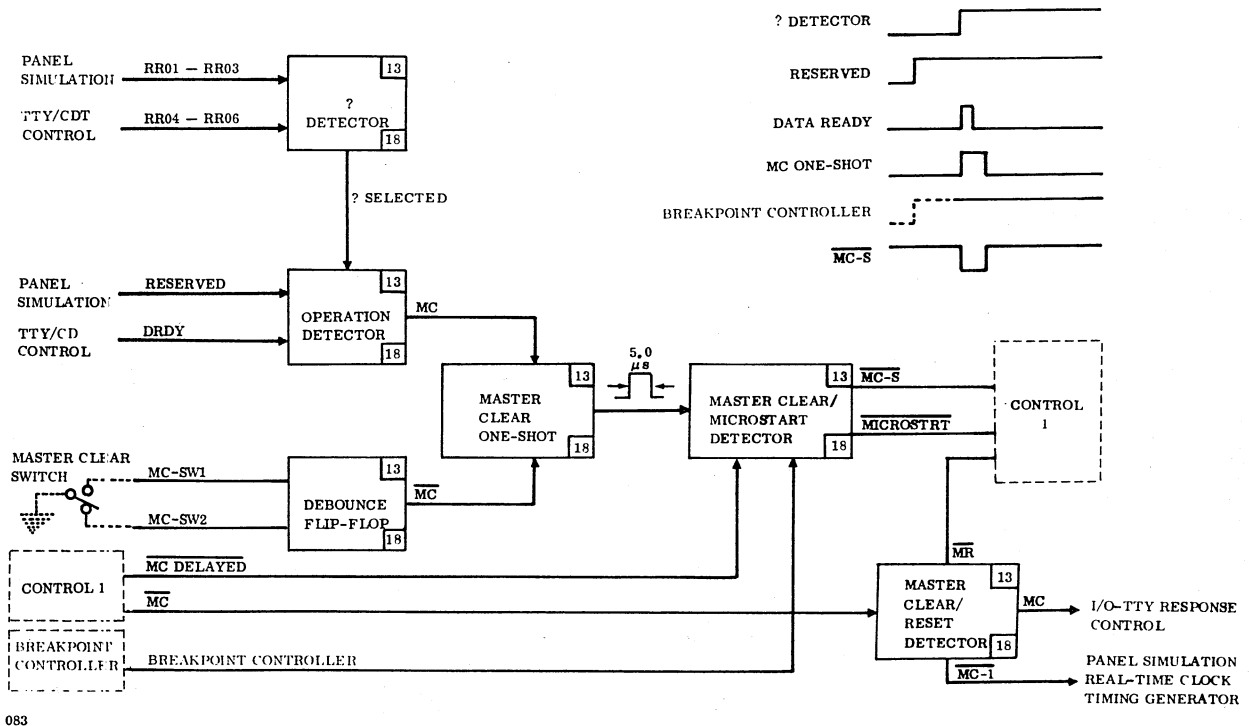


NOTE:

- - - INDICATES DON'T CARE CONDITIONS

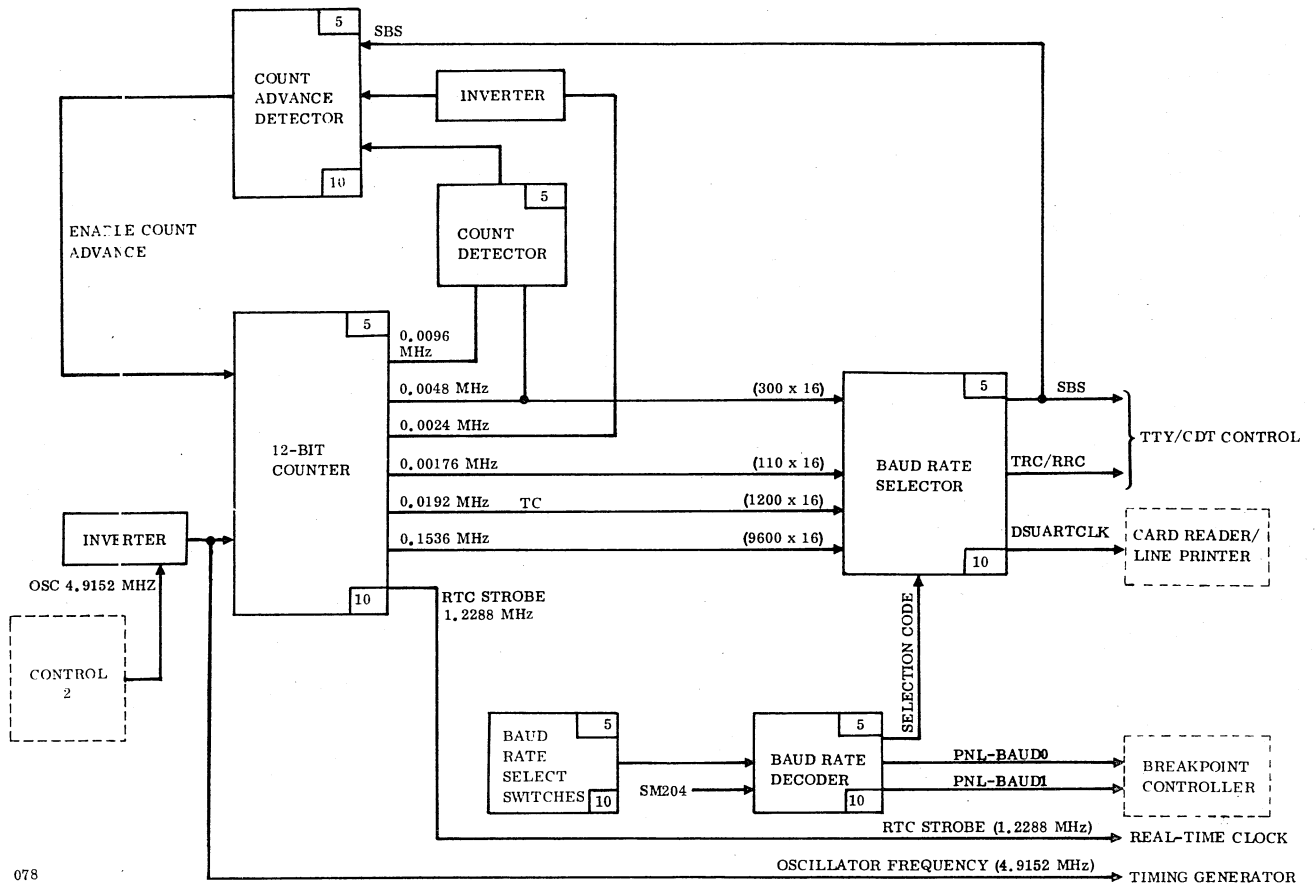
0118

Figure 4-17. Real-Time Clock Timing Sequence



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Figure 4-18. Master Clear/Microstart Function



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Figure 4-19. Baud Rate Generator Function

0.00176 MHz (110 x 16). These clock frequencies (9600 x 16), (1200 x 16), (300 x 16), and (110 x 16) are applied to the B inputs of selector (B6) [J6].

TABLE 4-10. BAUD RATE CLOCK FREQUENCY SELECTION

Clock Frequency (Hertz)	Baud Rate	Deadstart Select Segment Number		Program Select Segment Number	
		ON	OFF	ON	OFF
1,760	110	1 and 2	-	3 and 4	-
4,800	300	1	2	3	4
19,200	1200	2	1	4	3
153,600	9600	-	1 and 2	-	3 and 4

The applicable baud rate clock frequency is selected through proper setting of the baud rate select switch (S1) [SW1] segments 1, 2, 3, and 4 (table 4-11). These switches apply lows to the inputs of decoder multiplexer M11. When (M11) [M3] is set by SM204 being high, the deadstart baud rate selection signals PNLBAUD0 and PNLBAUD1 are sent to the breakpoint controller. The enable state select status is applied to S0 and S1 of selector (B6) [J6] to choose the clock frequency that appears at the QB and  $\overline{QB}$  terminals of selector (B6) [J6]. When the 110 x 16 baud rate frequency is selected, the QA output is high, and a high applied to the UART SBS input enables the selection of two stop bits per character code. All other baud rate frequencies produce a low at QA to select one stop bit per character code.

TABLE 4-11. BAUD RATE CLOCK FREQUENCY AND STOP BIT SELECTION

Frequency (Hertz)	S1	S0	Baud Rate	Stop Bits
1,760	0	0	110	2
4,800	0	1	300	1
19,200	1	0	1200	1
153,600	1	1	9600	1

The QB output of (B6) [J6] is buffered through AND gate (C2) [J8] to the UART to provide the transmit clock frequency (TRC) and the receive clock frequency (RRC). The complement of the QB output appears at the  $\overline{QB}$  output, which provides the deadstart UART clock signal DSUARTCLK to the panel interface.

TIMING GENERATOR FUNCTION

The timing generator (see figure 4-20) provides the basic timing required by the I/O-TTY controller. It provides the T1, T2, T3, and  $\overline{T3}$  timing pulses (figure 4-21) for the reply, reject, read mode, printer connected, character input, clear interrupt, and TTY-ADT-INT signals. All timing signals are generated by the 4.9152 MHz crystal-controlled oscillator signal received from the control 2 module via the baud rate generator. When the CPU read or write signals request an output or input operation, a reply occurs within a minimum of 200 nanoseconds and a maximum of 10 microseconds if the peripheral is ready to respond.

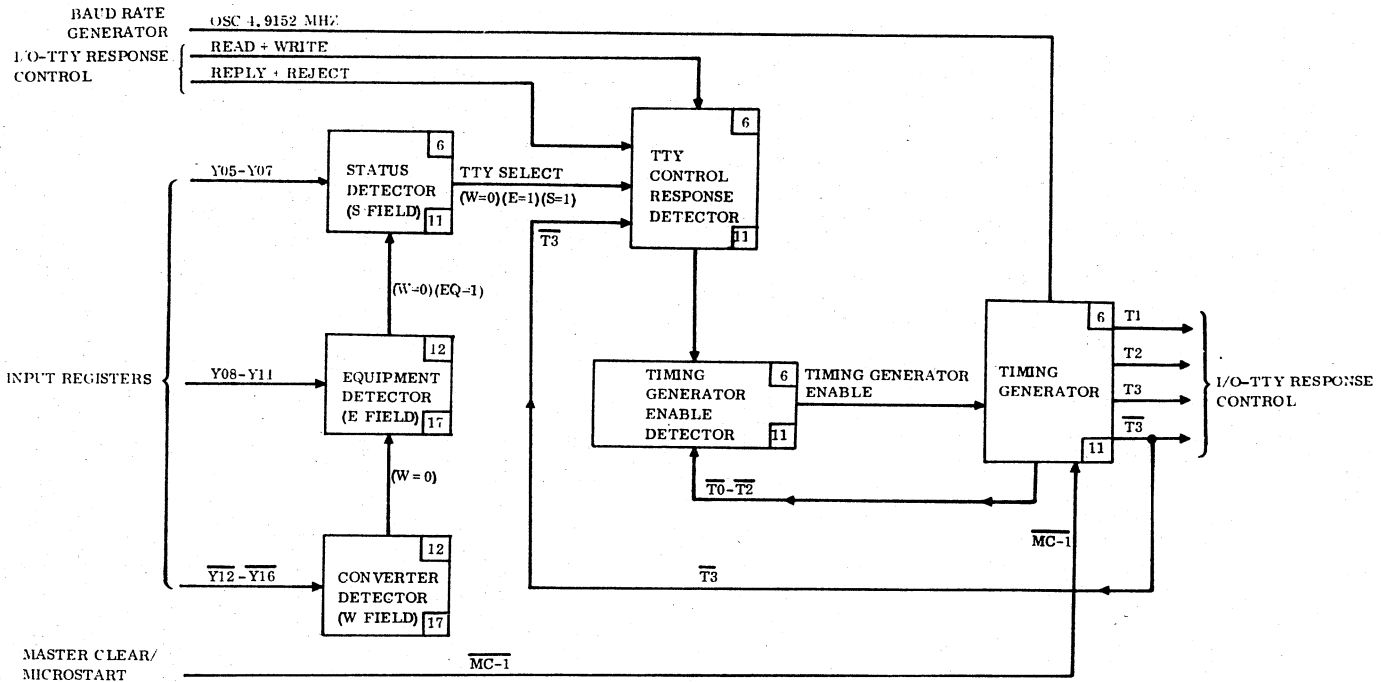


Figure 4-20. Timing Generator Function

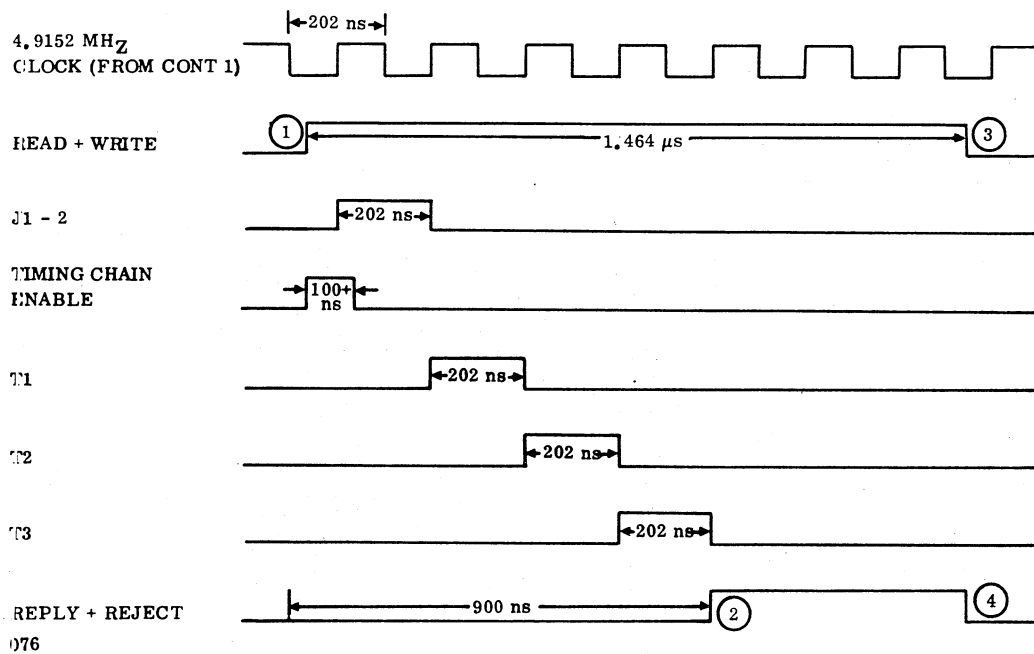


Figure 4-21. I/O-TTY Controller Timing Chart

If the peripheral is not ready to respond, a reject signal is returned within a minimum of 200 nanoseconds and a maximum of 10 microseconds. The timing generator initiates the sequences required to time these responses.

The converter, equipment, and status detectors decipher the Y-register address bits to determine that the TTY select code exists. The converter detector deciphers bits Y12 through Y16 to determine that the W=0 condition is present and couples the logic condition to the equipment detector. The W=0 condition is combined with bits Y08 through Y11 to develop the E field condition of E=1. This (W=0)(E=1) condition is applied to the status detector and combined with bits Y05 through Y07 to determine the (W=0)(E=1)(S=1) conditions.

When this is true, the TTYSEL high, REPLY+REJECT high, and T3 high are ANDed with the READ+WRITE high output of inverter (E5)[E1] at response detector AND gate (C4) [H1] and provide a high to (C4) [H1] pin 5. If all the Q outputs (except T3) of the four-bit shifter (B4) [J1] are high at (C4) [H1] pins 1, 2, and 4, the timing chain enabled signal is generated and applied to the D (pin 5) input of the shifter (B4) [J1]. This input creates a 202-nanosecond pulse at the Q (pin 2) output coincident with the rise of the oscillator (clock) frequency applied to CP of (B4) [J1]. This pulse triggers a chain reaction to generate the T1, T2, and T3 outputs (T1 triggers T2, which triggers T3). When T3 is high, the reply/reject flip-flop is latched to produce the REPLY+REJECT signal. The REPLY+REJECT high signal disables the time generator and remains high until the READ+WRITE signal drops coincident with the negative swing of the clock pulse. Also note that the timing chain

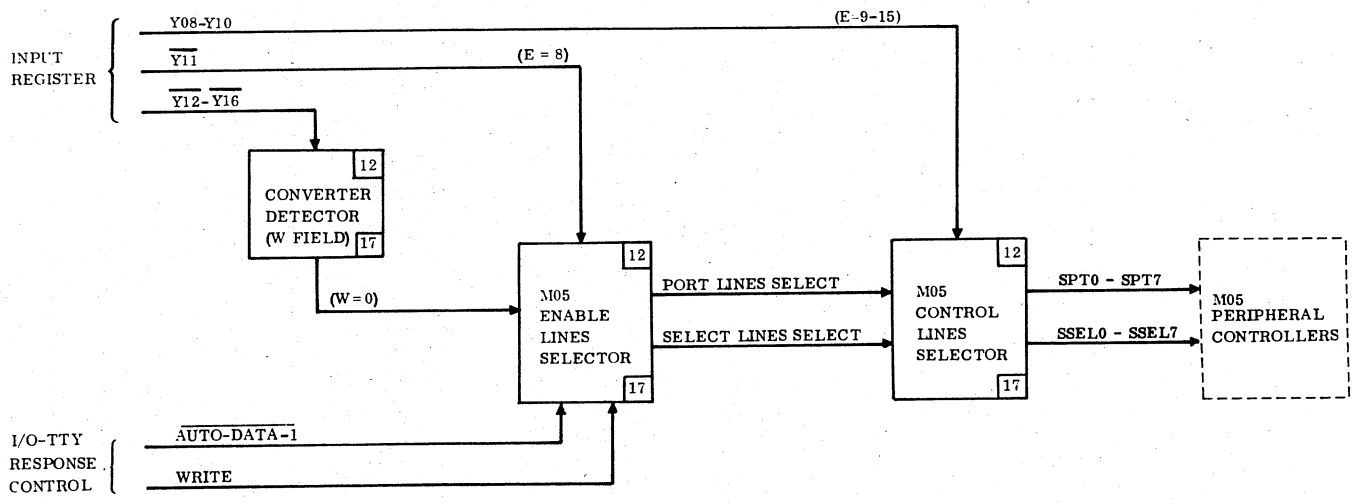
can be interrupted (aborted) anytime that a MC-1 low signal is applied to the clear input of the four-bit shifter.

#### M05 SET/SAMPLE FUNCTION

This function (see figure 4-22) provides eight port addressing (SPT0 through SPT7) lines and an eight-way parity selection scheme (SSEL0 through SSEL7). Each port is numbered 0 through 7 but designated 1 through 8 (that is, 0=1, 1=2, 2=3, etc.). Port 8 has the lowest priority. Each port can communicate with a peripheral directly or it may be multiplexed to communicate with up to eight peripherals. This provides for control of up to 64 peripherals (table 4-12). The multiplexed priority (scanning) scheme must be provided from an external means.

#### M05 Set-Sample Selection

The selector multiplexer designates which lines are active by the status of Y-register bits 8 through 11. Whenever the M05 capability is selected, Y11 is set high and when AUTO-DATA is high, these inputs are ANDed and inverted to place a low at the E inputs of multiplexer (M8) [M10]. If Y10 (the D input) is low, one of lines SSEL0 through SSEL7 is selected by the status of the four-position code applied to the S0 and S1 inputs by Y8 and Y9, respectively. Under these conditions, when both D and E are low, SSEL4 through SSEL7 are selected as S0 and S1 change to state 00, 10, 01, and 11, respectively. When D is high and E is low, SSEL0 through SSEL3 are selected as S0 and S1 change to state 00, 10, 01, and 11, respectively.



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Figure 4-22. M05 Set/Sample Selection Function

TABLE 4-12. M05 SET/SAMPLE SELECTION

Direct I/O Connection		Multiplexed I/O Connections							
		SPOS01, 02, and 03 Octal Code Equals							
Bit	Port	0	1	2	3	4	5	6	7
SPT00	0	1	9	17	25	33	41	49	57
SPT01	1	2	10	18	26	34	42	50	58
SPT02	2	3	11	19	27	35	43	51	59
SPT03	3	4	12	20	28	36	44	52	60
SPT04	4	5	13	21	29	37	45	53	61
SPT05	5	6	14	22	30	38	46	54	62
SPT06	6	7	15	23	31	39	47	55	63
SPT07	7	8	16	24	32	40	48	56	64

TABLE 4-13. SPT AND SSEL LINE SELECTION

Select Lines	S0/Y8	S1/Y9	Y10
SPT00, SSEL00	0	0	0
SPT01, SSEL01	1	0	0
SPT02, SSEL02	0	1	0
SPT03, SSEL03	1	1	0
SPT04, SSEL04	0	0	1
SPT05, SSEL05	1	0	1
SPT06, SSEL06	0	1	1
SPT07, SSEL07	1	1	1

Y register W-field bits Y13 through Y16 ( $\bar{Q}$  high outputs from flip-flops H11) are ANDed at (J10) [F7]. The resultant high is then ANDed with Y12 high at (G6) [H10] to produce W=0. This provides a low that is inverted (G7) [H8] for ANDing with Y11 and WRITE/ at AND gate (L4) [L9]. The Y11 and AUTO-DATA/ signals, if high at (L9) [L10], initiate the send line selection. The Y11, WRITE/, and W=0 conditions all high at (L4) [L9] initiate the send port line selection. With the selection condition initiated, the states of Y8, Y9, and Y10 activate the output selection when Y10 is high and the S0 and S1 code selects the particular output line. (Refer to table 4-13.)

All data is transferred from the processor to the peripheral device by the I/O set command (SMB09=1) and from the peripheral device to the processor by the I/O sample command (SMB09=0). Therefore, when the set condition exists, 16 bits of data (SD01 through SD16) are transferred from the D register onto the output lines. When the sample condition exists, 16 bits of data (RD01 through RD16) on the input lines are transferred to the main three-state bus (BUS01 through BUS16). When M05-type I/O controllers are employed, special signal wiring is required.

### EXTERNAL/INTERNAL SIGNAL GLOSSARY

Table 4-14 is a glossary of external data signals and table 4-15 is a glossary of internal control signals.

TABLE 4-14. EXTERNAL SIGNAL GLOSSARY

Term	Definition	Term	Definition
ADR01 through ADR16	Address data lines	MULTIND	Multilevel indirect addressing mode
AUTO-DATA/	Auto-data transfer	MULTINDPNL	Multilevel indirect addressing mode, panel selection
BUS00 through BUS15	Bus lines for transfer of data to CPU three-state bus	OSC 4.9152	Oscillator frequency 4.9152 MHz
CHARINPUT/	Character input	PNL-BAUD0	Baud rate selection for breakpoint controller baud rate generator
CPU-EDS/	CPU early data strobe	PNL-BAUD1	Baud rate selection for breakpoint controller baud rate generator
CPU-PROT/	CPU protect	PNLKEYINT/	Breakpoint controller keyboard (RDINT12/)
DATAINT8/	Data interrupt (RDINT08/)	PNLMODENA	Allows entering into the reserve (panel) mode when the escape button on the TTY/CD is pressed.
DS-SWNC	Deadstart switch, normal closed contact	PNLPRES/	Breakpoint controller present
DS-SWNO	Deadstart switch, normal closed contact	PNL-TTLOUT	Breakpoint controller TTL level output signal
DSUARTCLK	Deadstart universal asynchronous receive transmit clock	PROG-PROT/	Program protect
ENABLEIO	Enable input/output	PROTECT/	Protect
ENMMWRITE	Enable micro memory write	PROT-PNL1	Protect breakpoint controller
ENMMWRITEPNL	Enable micro memory write from the panel interface	RDINT01/	I/O-TTY controller auto-data transfer interrupt (TTY-ADT-INT1)
EXSTOP/	External stop	RDINT08	Data interrupt (DATAINT8)
GATEIOADR/	Gate I/O controller address	RDINT12/	Breakpoint controller keyboard interrupt (PNLKEYINT1)
GATEIODAT/	Gate I/O controller data	RDINT13	Breakpoint controller transmit buffer register empty interrupt (PNLTBRINT)
I/O-TTYIN	I/O-TTY controller input from teletypewriter	RD01/ through RD16	Read data from peripheral I/O controllers
I/O-TTYOUT	I/O-TTY controller output to teletypewriter	READ-SSTB/	Send strobe from CPU, which develops the read condition (input to CPU) (SSTB/)
MC/	Master clear	REJECT/	Reject (RPOS03/)
MCDELAYED/	Master clear delayed	REPLY/	Reply (RPOS02/)
MC-S/	Master clear set	RESYNC-I/O	Resynchronize input/output response
MC-SWNC	Master clear switch, normal closed contact	RPINT17/	Program interrupt
MC-SWNO	Master clear switch, normal open contact	RPINT24/	Program interrupt for RTC sequence (PROGINT/)
MICROSTRT/	Microstart	RS232IN-1	Console display (CD) or any RS232-C compatible device input
MIR12-	Micro instruction register output bit 12	RS232IN-2	
MI-SWNC	Manual interrupt switch, normal closed contact		
MI-SWNO	Manual interrupt switch, normal open contact		
MR/	Master reset		

TABLE 4-14. EXTERNAL SIGNAL GLOSSARY (Contd)

Term	Definition	Term	Definition
RS232OUT-1 RS232OUT-2	Console display (CD) or any RS232-C compatible device output	SM212/	Status mode bit 212 (initiate panel simulation panel mode)
RTERM	Receive termination	SPT0 through SPT7 <sup>†</sup>	Send port line
SD01 through SD16	Send data line to peripheral I/O controllers	SSEL0 through SSEL7 <sup>†</sup>	Send select line
SELGETMAK/	Select	STERM/	Send terminate (RTC sequence and end of page status)
SELSKIP/	Selective skip	S300/ through S315/	Data input lines from CPU arithmetic logic unit (ALU) S3
SELSKIPNL/	Selective skip from breakpoint controller	TTL-SRL	TTL serial input
SELSTOP	Selective stop	TTL-SRL2/	TTL serial output
SELSTOPPNL/	Selective stop from breakpoint controller	TTY-ADT-INT/	I/O-TTY controller auto-data transfer interrupt (RDINT01)
SETSM204/	Set status mode bit 204 (deadstart loading)	TTYUARTOUT	Teletypewriter UART output (character data from UART to teletypewriter)
SM204/	Status mode bit 204 (initiate deadstart loading)	WE0	W equals zero (W field of address word bit Y12 through Y16, are all low)
SM210	Status mode bit 210 (initiate panel simulation data ready reset for UART)	WRITE/	Write (output from CPU)
SM211/	Status mode bit 211 (initiate panel simulation transmit buffer loading of UART)		

<sup>†</sup>Designations applicable to M05 set/sample capability only when custom-wired.

TABLE 4-14. EXTERNAL SIGNAL GLOSSARY

Term	Definition	Term	Definition
ADR01 through ADR16	Address data lines	MULTIND	Multilevel indirect addressing mode
AUTO-DATA/	Auto-data transfer	MULTINDPNL	Multilevel indirect addressing mode, panel selection
BUS00 through BUS15	Bus lines for transfer of data to CPU three-state bus	OSC 4.9152	Oscillator frequency 4.9152 MHz
CHARINPUT/	Character input	PNL-BAUD0	Baud rate selection for breakpoint controller baud rate generator
CPU-EDS/	CPU early data strobe	PNL-BAUD1	Baud rate selection for breakpoint controller baud rate generator
CPU-PROT/	CPU protect	PNLKEYINT/	Breakpoint controller keyboard (RDINT12/)
DATAINT8/	Data interrupt (RDINT08/)	PNLMODENA	Allows entering into the reserve (panel) mode when the escape button on the TTY/CD is pressed.
DS-SWNC	Deadstart switch, normal closed contact	PNLPRES/	Breakpoint controller present
DS-SWNO	Deadstart switch, normal closed contact	PNL-TTLOUT	Breakpoint controller TTL level output signal
DSUARTCLK	Deadstart universal asynchronous receive transmit clock	PROG-PROT/	Program protect
ENABLEIO	Enable input/output	PROTECT/	Protect
ENMMWRITE	Enable micro memory write	PROT-PNL1	Protect breakpoint controller
ENMMWRITEPNL	Enable micro memory write from the panel interface	RDINT01/	I/O-TTY controller auto-data transfer interrupt (TTY-ADT-INT1)
EXSTOP/	External stop	RDINT08	Data interrupt (DATAINT8)
GATEIOADR/	Gate I/O controller address	RDINT12/	Breakpoint controller keyboard interrupt (PNLKEYINT1)
GATEIODAT/	Gate I/O controller data	RDINT13	Breakpoint controller transmit buffer register empty interrupt (PNLTBRINT)
I/O-TTYIN	I/O-TTY controller input from teletypewriter	RD01/ through RD16	Read data from peripheral I/O controllers
I/O-TTYOUT	I/O-TTY controller output to teletypewriter	READ-SSTB/	Send strobe from CPU, which develops the read condition (input to CPU) (SSTB/)
MC/	Master clear	REJECT/	Reject (RPOS03/)
MCDELAYED/	Master clear delayed	REPLY/	Reply (RPOS02/)
MC-S/	Master clear set	RESYNC-I/O	Resynchronize input/output response
MC-SWNC	Master clear switch, normal closed contact	RPINT17/	Program interrupt
MC-SWNO	Master clear switch, normal open contact	RPINT24/	Program interrupt for RTC sequence (PROGINT/)
MICROSTRT/	Microstart	RS232IN-1	Console display (CD) or any RS232-C compatible device input
MIR12-	Micro instruction register output bit 12	RS232IN-2	
MI-SWNC	Manual interrupt switch, normal closed contact		
MI-SWNO	Manual interrupt switch, normal open contact		
MR/	Master reset		

TABLE 4-14. EXTERNAL SIGNAL GLOSSARY (Contd)

Term	Definition	Term	Definition
RS232OUT-1 RS232OUT-2	Console display (CD) or any RS232-C compatible device output	SM212/	Status mode bit 212 (initiate panel simulation panel mode)
RTERM	Receive termination	SPT0 through SPT7 <sup>†</sup>	Send port line
SD01 through SD16	Send data line to peripheral I/O controllers	SSEL0 through SSEL7 <sup>†</sup>	Send select line
SELGETMAK/	Select	STERM/	Send terminate (RTC sequence and end of page status)
SELSKIP/	Selective skip	S300/ through S315/	Data input lines from CPU arithmetic logic unit (ALU) S3
SELSKIPNL/	Selective skip from breakpoint controller	TTL-SRL	TTL serial input
SELSTOP	Selective stop	TTL-SRL2/	TTL serial output
SELSTOPPNL/	Selective stop from breakpoint controller	TTY-ADT-INT/	I/O-TTY controller auto-data transfer interrupt (RDINT01)
SETSM204/	Set status mode bit 204 (deadstart loading)	TTYUARTOUT	Teletypewriter UART output (character data from UART to teletypewriter)
SM204/	Status mode bit 204 (initiate deadstart loading)	WE0	W equals zero (W field of address word bit Y12 through Y16, are all low)
SM210	Status mode bit 210 (initiate panel simulation data ready reset for UART)	WRITE/	Write (output from CPU)
SM211/	Status mode bit 211 (initiate panel simulation transmit buffer loading of UART)		

<sup>†</sup>Designations applicable to M05 set/sample capability only when custom-wired.

TABLE 4-15. INTERNAL CONTROL SIGNAL GLOSSARY

Term	Definition	Term	Definition
ADT-SELECTED	Auto-data transfer selected	MC-1	Master clear 1; internal I/O-TTY controller master clear derived from the applied external MC signal
CHAR INPUT	Character input (response control to indicate a character code is ready for read to CPU)	P.E.	Parity error; parity bit indicates received character code word is incorrect
CLR-CONT+CLR-INT	Clear controller or clear interrupt; clear I/O-TTY controller or clear interrupt from I/O-TTY controller)	PROT	Protect; condition requires that the response to the CPU affect a protected area of memory
D01 through D16	Data bits from D register that are employed within the I/O-TTY controller	PNLPRES	Breakpoint controller present; indicates whether the breakpoint controller is inserted
DRDY	Data ready and BEL code; manual interrupt application from character code generator	PSIM-DRR	Panel simulation data receive reset; reset to UART receive register to enable input of new character code
(DRDY) (BEL-ESC +RES • PP)	Data ready and BEL or escape or reserved and breakpoint controller present; special character codes for selection of manual interrupt, release reserve, reserve when panel mode is selected	PSIM-ECHO	Breakpoint controller (panel simulation) echo; selection of echo response to output device in a panel mode operation
DRR	Data received reset; enables loading of UART receive register	PSIM-TBRL	Panel simulation transmit buffer register load; loading of UART transmit buffer register during panel simulation mode
(DS) (DIR-RT)	Data status and director	READ	Command from CPU requesting an input response
E-REPLY	Enable reply; initiates enable of the I/O-TTY controller reply response to the CPU	READMODE	Indicates the read mode condition of I/O controllers has been enabled
E-TTYREPLY	Enable I/O-TTY controller reply response to the CPU	REJECT	Response control signal to advise CPU the I/O-TTY controller is not available to write or read data
EOPSTATUS	End of page status; message termination has taken place at end of page	RELEASED	Provide for release of reserved condition, panel mode
FERROR	Framing error; character code received contained an error of start, data, parity or stop format	REPLY	Response control signal to advise CPU the I/O-TTY controller has provided write or read data
HI-1, -2, -3	High input (common tie point 1, 2, or 3 for a logic high termination)	RR1 through RR8	Receiver register data bits 1 through 8; character code data bits from UART to the CPU and internal I/O-TTY controller logic
INT STATUS	Interrupt status; indicates to CPU that interrupt exists	RESERVED	Provides for breakpoint controller panel mode operation
K MODE	Keyboard mode (printer connected)	RTCSEL	Real-time clock selected; enables real-time clock logic
KMODE • REMODE	Keyboard mode and read mode; read mode is enabled and printer is connected	SELTTYSTATUS	Select TTY status; enables the I/O-TTY controller status to be placed on the CPU three-state bus
MANINTSTATUS	Manual interrupt status; indicates to the CPU that a manual interrupt has occurred		

TABLE 4-15. INTERNAL CONTROL SIGNAL GLOSSARY (Contd)

Term	Definition	Term	Definition
STROBE-D	D-register strobe to check data from CPU ALU to D register flip-flop	UART-IN	Universal asynchronous receiver transmitter input; input to the UART from the teletypewriter, CD, or break-point controller
T1, T2, T3	Timing pulses produced by internal timing generator	WRITE	Command from CPU that output is ready
TBEMPTY	The UART transmit buffer register is empty	WT-MODE	The write mode condition of peripheral I/O controllers has been enabled
TERM	Terminates RTC sequence and TTY busy status	(W=0) (EQ=1)	W equals zero and E equals one; conditions derived from Y register address bits
TREEMPTY	The UART transmit register is empty	(XXXX X111)	RR1, RR2, RR3 are high (1s) and RR4 through RR7 are immaterial
TTY-DRR	TTY data receive reset; initiates the UART data receive reset	Y01 through Y16	Address word bits from Y register used by internal I/O-TTY controller logic
TTYSEL	TTY select; initiates the response from the I/O-TTY controller	1.2288 MHz	Basic clock frequency for generating the real-time clock 3.3 millisecond time pulses
TTY-TBRL	TTY transmit buffer register load; initiates loading of the UART transmit buffer register		

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The logic diagrams for the I/O-TTY controller are contained in the field print package.

This section of the manual contains diagrams that show the connections between the I/O-TTY controller, the

teletypewriter, the console display, the peripheral I/O controllers, and the CPU.

Figure 5-1 shows the external data signal lines for the I/O-TTY controller, and figure 5-2 gives the external control lines.

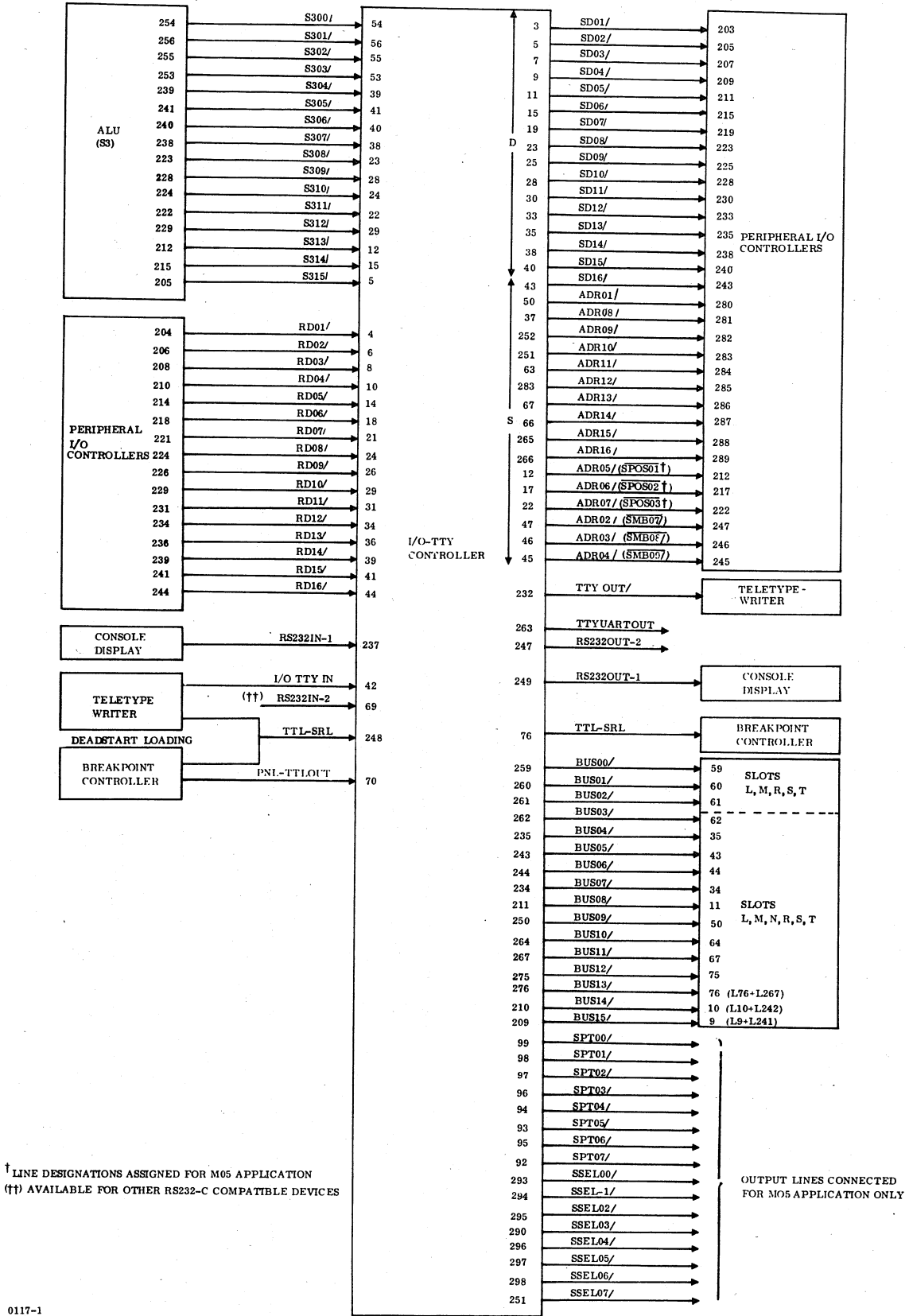


Figure 5-1. External Data Signal Lines

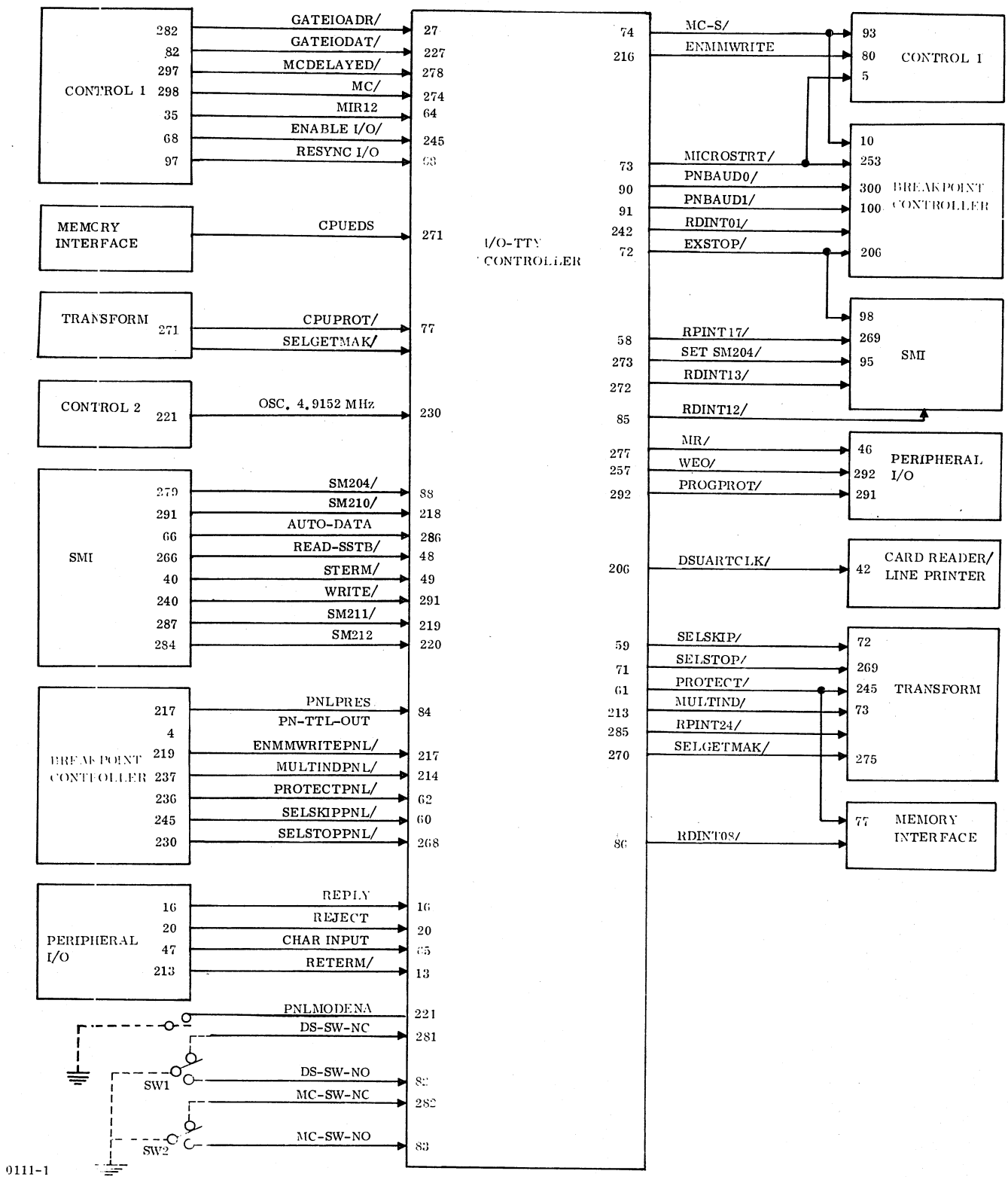


Figure 5-2. External Control Signal Lines



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## MAINTENANCE

Both emergency and preventive on-site maintenance is limited to isolating a fault to the replaceable subassembly, then effecting repair by replacing the faulty assembly with a previously tested spare.

### CAUTION

The I/O-TTY PWA contains electrostatic-sensitive devices and is identified with a red solder mask. Exercise extreme care in handling to avoid damage. Common practices, such as touching a grounded surface before handling, inserting in anti-static or conductive bags for storage or transfer, repairing at only properly equipped and grounded work stations, etc., must be strictly followed.

## SPARES TESTING

All spare subassemblies must be tested upon receipt, with retesting occurring annually.

## PREVENTIVE MAINTENANCE

No preventive maintenance is required for the I/O-TTY controller.



COMMENT SHEET

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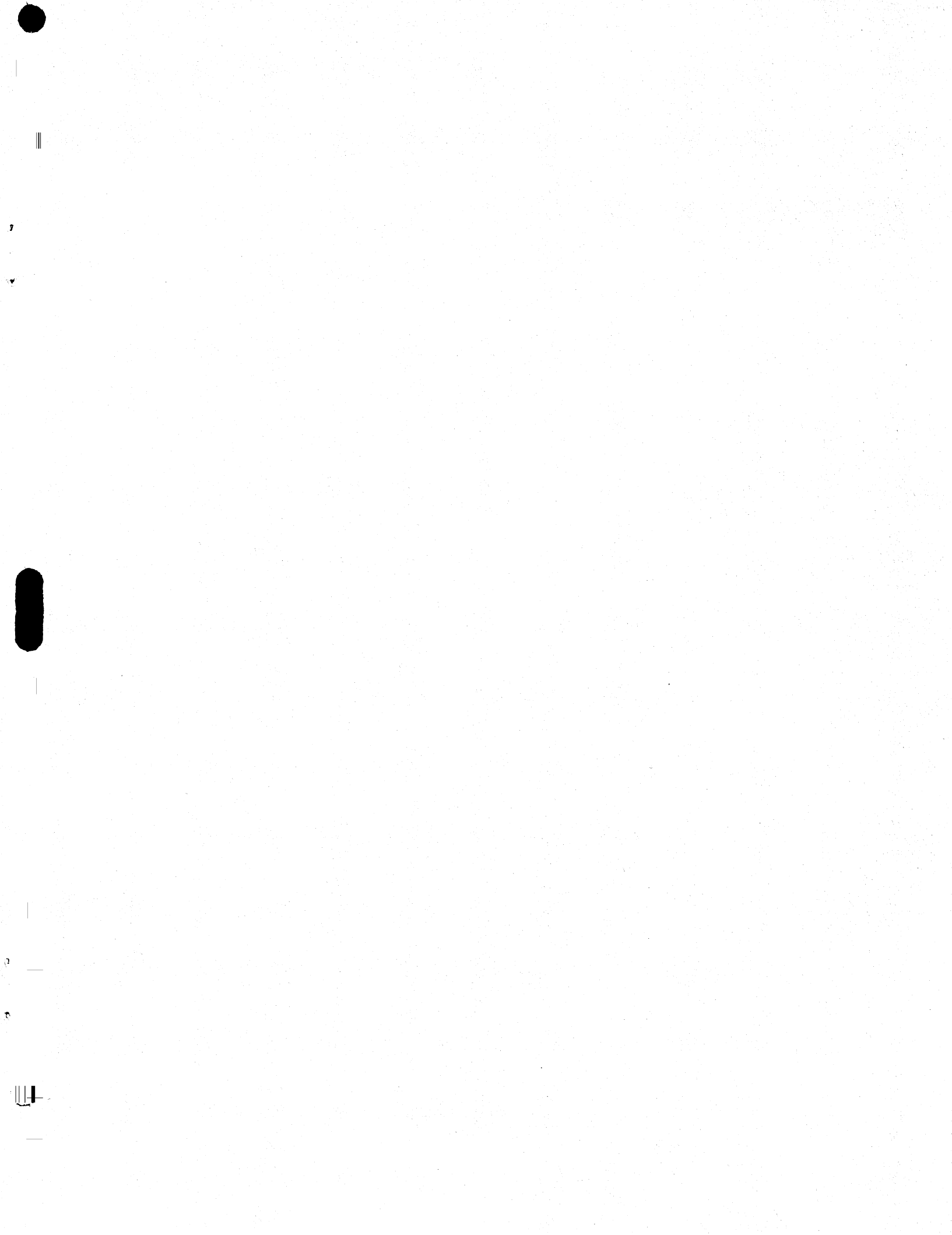
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